SynTest Technologies

The *Testability* Company

@Speed

SynTest's Quarterly Newsletter
July 2006 Vol. 2

Welcome to the July issue of the @Speed. This quarterly e-Newsletter gives you the latest news about SynTest corporation, products and solutions. For comments and suggestions, please contact info@syntest.com.

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DAC 2006 is around the corner……

This year DAC 2006 will be held July 24-28 at San Francisco Moscone Center, CA, USA.
SynTest Exhibit BOOTH# is 1022.
We cordially invite you all to visit our booth

What is new from SynTest @DAC 2006……..

Going Hierarchical – SynTest's flagship DFT products, VirtualScan and TurboBIST-Logic, now offer a hierarchical DFT logic incorporation feature to allow IP suppliers as well as SoC design houses to implement the said DFT technology for individual blocks then integrate those blocks at chip-top. The tools are called Hierarchical VirtualScan and Hierarchical TurboBIST-Logic respectively, or HVS and HTBL for short. For integration at chip-top, the tool offers a solution to test the glue logic for faults between the blocks.

Users can use HVS with or without isolation wrappers around the blocks. The blocks can have a mixture of VirtualScan or full-scan DFT. For small blocks, some users prefer to not have compression to save logic overhead. Users can also elect to apply tests to all blocks at once or sequentially.

For HTBL, due to the nature of the logic BIST technology, each block is fully "wrapped" making each an autonomous, fully self-testable block. The TAP controller at chip-top integrates all the HTBL blocks and allows users flexibility to schedule their respective test sessions. Users may opt to not test all the blocks at once to avoid excessive power or noise dissipation during test.

This divide-and-conquer approach enables project management to easily manage multiple design teams responsible for sub-circuit(s) of one single IC. It empowers individual design team to meet their DFT requirements and at the same time contributing to overall DFT goal of the end product.

VLSI TEST PRINCIPLES AND ARCHITECTURES

Design for Testability (First Edition)
By Laung-Terng Wang, SynTest Technologies, Inc., Sunnyvale, CA, USA.
Cheng-Wen Wu, National Tsing Hua University, Hsinchu, Taiwan.
Xiaoqing Wen, Kyushu Institute of Technology, Fukuoka, Japan.

Is available now. Please visit http://elsevier.com/inca/707926 for more information and to purchase the book.
SynTest DFT tools will be available for download from July 7, 2006 when the textbook is purchased.

SynTest Engineers were busy publishing Technical Articles ....

A New ATPG Method for Efficient Capture Power Reduction During Scan Testing

X. Wen, S. Kajihara, K. Miyase, T. Suzuki, K. K. Saluja, L.-T. Wang, K. S. Abdel-Hafez, and K. Kinoshita, 24th IEEE VLSI Test Symposium, 2006.

Abstract

High power dissipation can occur when the response to a test vector is captured by flip-flops in scan testing, resulting in excessive IR drop, which may cause significant captureinduced yield loss in the DSM era. This paper addresses this serious problem with a novel test generation method, featuring a unique algorithm that deterministically generates test cubes not only for fault detection but also for capture power reduction. Compared with previous methods that passively conduct X-filling for unspecified bits in test cubes generated only for fault detection, the new method achieves more capture power reduction with less test set inflation. Experimental results show its effectiveness.

Please send an email to support@syntest.com to request a copy of this paper.

Updates on Patents Approvals

SynTest Patents Portfolio is getting rich steadily. 5 patents have been issued so far:

Staggered skewed-load (U.S. Pat. No. 6,954,887)
Staggered double-capture (U.S. Pat. No. 7,007,213)
DFD & yield Improvement (U.S. Pat. No. 7,058,869)
RTL scan synthesis (U.S. Pat. No. 6,957,403)
X-mask network design (U.S. Pat. No. 7,032,148)

2 patents are allowed so far: DFD for scan cores (European patent) and Smart ATPG

Patents for VirtualScan and UltraScan are pending and should be approved any time in second half of this year.

Let Distributed ATPG save your precious time

By David Wang, Applications Engineering

SynTest ATPG can reduce the turn around time (TAT) by distributing tasks across multiple CPUs for very large and complex designs. Users can choose clock grouping or fault lists partition to create multiple ATPG tasks. Our customers' experiments showed that when using 5 CPUs, the TAT was reduced 4x times for the same Fault Coverage. When using 12-16 CPUs, ATPG in the distributed mode can be accelerated by a factor of 10. After running distributed ATPG, users can merge all distributed patterns and run fault simulation to do fault grading and perform static pattern compaction to further reduce pattern counts by approximately 10% to 40%. The distributed ATPG supports all fault models: stuck-at, transition, bridging and Iddq.

Since transition faults required much longer TAT than stuck-at faults, if the circuit is over 4M gates, customers need to consider the distributed ATPG for transition faults. We suggest customers to use clock grouping and distribute the different groups on different CPUs since clock grouping is more effective than fault lists partition. The experiments show that clock grouping also has the advantage of minimizing the pattern counts and TAT.

Try to use SynTest distributed ATPG now. It can save your precious time in your design cycle and lower the overall cost of test. DFT IP Licensing scheme from SynTest includes a site license with *unlimited* copies of tools to allow customers to put this saving to work for you right away! If you have any question, please feel free to contact SynTest applications engineering groups. You can send email to support@syntest.com

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