



SYNTEST

*The Testability Company*

**T**oday, integrated chips with multi-million gates, containing logic, memory and analog functions are becoming common place. At the same time, controlling costs and maintaining high quality standards are critical to the success of any such new development. In such situations, fault simulation plays an important role in providing accurate fault coverage for areas not covered by scan or BIST.

### High Performance Fault Simulation

**TurboFault™** combines high performance, versatility and accuracy for classical test fault grading.

**TurboFault™** is the fastest concurrent fault simulator based on the latest advances in cycle-based simulation technology. It simulates even faster than existing expensive hardware-accelerated fault simulators.

**TurboFault™** supports synchronous and asynchronous designs at the gate level, including tri-state gates, latches, flip-flops, single and multi-port RAMs, complex bus resolution functions, and User Defined Primitives (UDPs). It reads Verilog or VHDL gate-level netlists, WGL patterns, VCD files as well as Standard Delay Format (SDF) timing files.

### Advanced Cached-Concurrent™ Algorithm

**TurboFault™** utilizes a new algorithm optimized for modern computer hardware that maximizes the power of today's workstations. SynTest Cached-Concurrent™ algorithm with the new Fast Queue™ technology combines the best of unit delay and cycle-based capabilities. The Cached-Concurrent™ operation reduces the number of gate evaluations; Fast Queue™ manages fault lists efficiently.

**TurboFault™** makes fault simulation an integral design tool for generating a quality manufacturing test set. TurboFault™ supports single timing delay for simulation accuracy and flexibility, without sacrificing speed.

**TurboFault™** reports faults as Hyperactive, Oscillatory, Hard Detect, Probably Detected, Potentially Detected, Undetected, or Uncompleted. Any or all of these can be combined in a single or in multiple reports which can be "wrapped around" as inputs for the next incremental fault simulation run, or passed to spreadsheets or plotting tools for analysis.

### Low Memory Consumption

Because fault simulation can consume memory very quickly, memory management is critical. TurboFault™ handles this by combining very efficient memory management, with special fault handling capability resulting in low memory consumption.

## WHY FAULT SIMULATION:

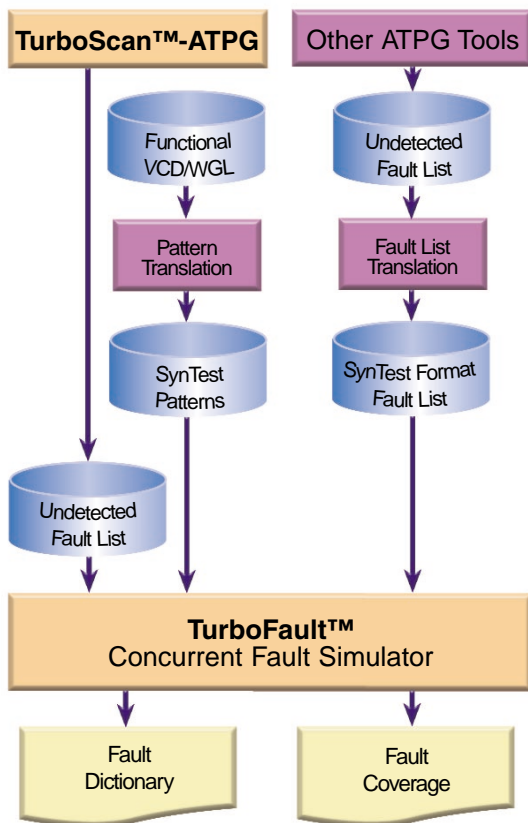
- To add some vectors to test logic not covered by scan or BIST, to check that test logic has been inserted correctly, or to understand and correct fault coverage problems.
- When using multiple instantiation of "legacy" logic circuit blocks or re-using IP cores in different designs, a way to check that the various embedded blocks and their vectors have been correctly glued together with the rest of the chip to produce a complete set of test vectors and a test program.
- To measure fault coverage and estimate defect levels in scan or BIST structures.
- To measure fault coverage in areas unreachable by scan or BIST structures, or where complete and reliable accuracy is required.
- To measure fault coverage in circuits where DFT insertion is not used due to the overhead, which would be added to the circuit, if DFT were to be used.
- Test engineers add empirically designed test vectors to catch certain manufacturing defects. Fault simulation can help determine the effectiveness of these additional test vectors in improving fault coverage.

## FEATURES OF TURBOFAULT™

- Uses cycle-based simulation technology
- Advanced Cached-Concurrent™ Algorithm
- Low memory consumption
- User Definable Fault Detection Criteria
- Fault Tracing Capability
- Crash Recovery Capability
- Offers Multi-Pass, Incremental Simulation and Distributed Processing
- Accepts various inputs including reports from SynTest's TurboScan™-ATPG tool as well as from other EDA vendors' ATPG tools.
- Offers a variety of reports/outputs, such as histograms, aggregated fault coverage reports, module level fault coverage reports, recommended list of patterns and a list of cut-off points.
- Supports toggle tests
- Flexible fault insertion points

## INPUTS TO TURBOFAULT™

- Gate-level cell library files in Verilog or VHDL, gate-level or transistor-level netlists
- SDF timing annotation file (if available).
- Test Patterns in Verilog or VHDL or mixed, VCD or WGL or FSDB (Debussy)
- Fault list/coverage report: Output from an Automatic Test Pattern Generator (if available)
- TurboFault™ can read in reports from Synopsys' TestGen/TetraMAX and Mentor FastSCAN tools, as well as from Zycad.



## Performance, Capacity, Flexibility

**TurboFault™** provides special handling for Oscillatory and Hyperactive faults. Oscillatory faults are handled using a window timer approach. Any faults that oscillate longer than the "window" time are considered oscillating and automatically dropped. Hyperactive faults are also detected internally and optionally dropped.

Functional test vectors are not the only component of the fault simulation. Many customers use an ATPG tool to generate additional test vectors for the faults undetected by the functional test vectors. By utilizing its powerful system simulation capabilities, TurboFault™ integrates and fault grades test programs from many sources. TurboFault accepts Verilog VCD, WGL, FSDB, and SynTest ATPG patterns as input stimuli.

## User Definable Fault Detection Criteria

**TurboFault™** allows a user to define the criteria for a fault in order for it to be declared as detected. This gives the simulator the highest flexibility to emulate many test environments and Automated Test Equipment. Faults can be inserted either on the cell boundary or at different levels as per users' requirements.

## Fault Tracing and Back Tracing Capability

**TurboFault™** can also be used as a simple diagnostic tool. The fault-tracing feature allows users to compare the circuit activities between faulty and normal chips. This can speed up tuning test vectors, isolating faulty circuits and debugging failed parts. Waveform data can be output in ASCII, VCD or FSDB (Debussy) formats.

## Crash Recovery Capability

**TurboFault™** not only provides first rate performance but also second-to-none reliability. The crash recovery function allows recovery of the simulation data and protects results from any environmental adversities, such as network glitches and power outages. This feature ensures the highest and fastest rewards from the investment of time and computation resources.

## Multi-Pass and Incremental Simulation

**TurboFault™** is intelligent enough to inspect the computer resources available and determine the optimal configuration for running a fault simulation job. If the number of faults is too large to fit into one computer at a time, TurboFault™ can partition the faults into separate groups and submit simulation tasks in multiple passes for each group. This automatic partitioning capability reduces the number of faults per pass and thus reduces paging. The results from different groups are then automatically merged in the final report.

Incremental simulation reduces the number of faults per run. A stimulus suite often consists of test pattern files where each pattern file requires a separate fault simulation session. Merging different fault-grading reports is a tedious and time-consuming effort. TurboFault™ provides an easy way to accumulate fault-grading results from different fault simulation sessions. This frees the user to focus on analyzing the overall result instead of struggling with sorting individual reports.

## User Interface & Library Modeling

**TurboFault™** is one of the first EDA tools to adopt the powerful Tcl (Tool Command Language) user interface. Fault simulation control cannot be easier or more intuitive. Complicated fault simulation control can be quickly implemented in Tcl scripts with most common UNIX shells constructs available. The Tcl interface supports both batch and interactive modes.

**TurboFault™** accepts gate-level cell descriptions and User Defined Primitives (UDPs). SynTest also provides a cell library builder to build gate-level models. The library is compatible across all SynTest tools, including TurboScan™-ATPG. TurboFault™ supports Verilog and VHDL gate-level and single timing models.

**TurboFault™** memory modeling provides basic memory building blocks for handling ROMs, and single and multi-port RAMs, either synchronous or asynchronous. Common memory model vendors, e.g. Artisan, Virage, are supported by SynTest's model generators.

## Concurrent Fault Simulation

Concurrent fault simulation is the most widely used fault-simulation algorithm and takes advantage of the fact that a fault does not affect the whole circuit.

Hence, in a concurrent fault simulation, we first completely simulate the good circuit. Then we inject a fault and re-simulate only that part of the circuit that behaves differently.

Keeping track of exactly which parts of the circuit need to be re-simulated for each new fault is complicated, but the savings in memory and processing that result allow thousands of faults to be simulated simultaneously.

A concurrent simulation is split into several blocks. You can usually control how many faults (usually around 10,000) are simulated in each block or pass. Each pass thus consists of a series of test cycles. Every circuit has a unique fault-activity signature that governs the divergence that occurs with different test vectors. Thus every circuit has a different optimum setting for faults per pass.

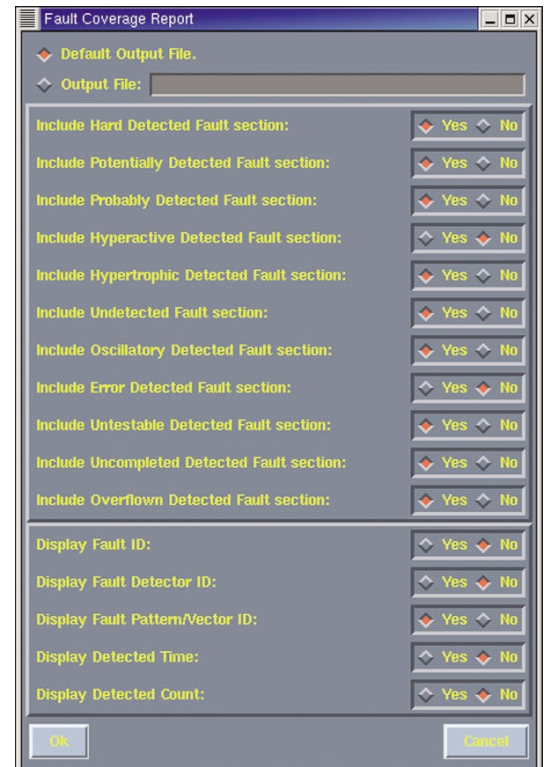
Too few faults per pass will not use resources efficiently. Too many faults per pass will result in memory overflow.

## Reporting

**TurboFault™** produces concise statistics and detailed reports on fault coverage, fault classifications, module level statistics and toggle tests.

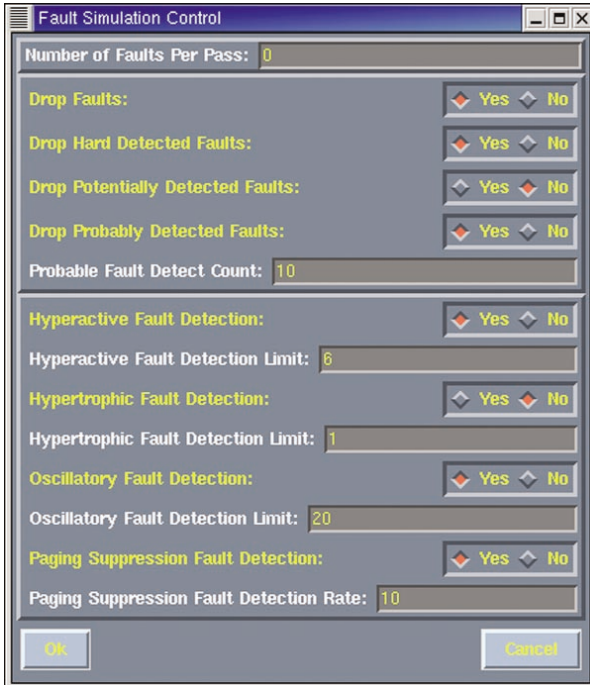
It reports faults as Hyperactive, Hypertrophic, Oscillatory, Hard Detect, Probably Detected, Potentially Detected, Undetected, or Uncompleted. Any or all of these can be combined in a single or in multiple reports which can be "wrapped around" as inputs for the next incremental fault simulation run, or passed to spreadsheets or plotting tools for analysis.

In addition, undetected faults can be passed directly to SynTest ATPG tools for additional processing.



## OUTPUTS FROM TURBOFAULT™

- A histogram that gives fault coverage changes along the time line for each pattern file.
- An aggregated fault coverage report which gives status of each potential defect/fault in the netlist. Pins and patterns that detect the fault can be reported as well.
- Module level fault coverage reports: Give the coverage numbers for each individual module.
- Module level toggle test reports.
- Recommended list of patterns and a list of cut-off points.



## Platforms

TurboFault™ runs on Sun Solaris, HP-UX and Linux operating PCs networked on an UNIX server.

## Distributed Processing

TurboFault™'s distributed processing capability enables it to assign jobs dynamically to various available machines and collect the results. If one machine fails, TurboFault™ will automatically re-assign the job to other available machines.

## ORDERING INFORMATION

**TurboFault™:** For Concurrent Fault Simulation

### Other Products from SynTest

- DFT-PRO™ (includes)
  - TurboBSD™: For Boundary-scan Synthesis
  - TurboBIST-Memory™: For Memory-BIST Synthesis
  - TurboDFT™: For DFT Integration
  - TurboCheck™: For DFT Rule Checking
  - TurboScan™-Synthesis: For Scan Synthesis
  - TurboScan™-ATPG: Automatic Test Pattern Generation
  - ATE Test Program Outputs (select 1 – for Agilent, Credence or Teradyne)
- TurboBIST-Logic™- Logic BIST Tool Suite
- TurboDebug™: For Debugging and Diagnosis of PCBs and SOCs.

## TurboFault™ – The Unique Fault Simulator

The mission of a fault simulator is to measure the quality of test patterns for any possible defects introduced in the chip manufacturing process. The patterns are simulated on the design by injecting an imaginary defect. If an erroneous output can be observed on the primary ports of the chip, it will be safe to assume that the defect will be detected by the same patterns in the real manufacturing test.

For millions of possible defects, there will be millions of logic simulation tasks to complete. To reduce this computation cost, many solutions have been proposed in the past 30 years. Their main focus has been on how to identify the redundancy among the millions of logic simulations and how to eliminate it.

Two approaches are widely adopted today:

- the concurrent simulation algorithm
- the differential simulation algorithm.

The concurrent simulation approach is believed to provide the most accurate results with full timing support. However, it falls short on the overall performance and memory consumption.

The differential simulation algorithm is good at handling combinational circuits but the overhead to deal with sequential logic may offset any performance advantage. Its application is often limited to pure synchronous designs while the concurrent algorithm is far more versatile.

**TurboFault™** is based on a brand-new fault simulation algorithm, which is basically a combination of the concurrent and the differential approaches.

The well-balanced design in its kernel allows it to keep the accuracy, flexibility, and circuit compatibility of the concurrent solution, while the application of the differential algorithm helps reduce the memory usage and improve the performance.

At the same time, a very fast gate-level logic simulation engine gives TurboFault™ a solid base to boost.

## Licensing

To enable users fully utilize the concurrent simulation capabilities, SynTest offers **TurboFault™** licenses as "Main" licenses and "Peak" licenses.

The Peak licenses can be procured for short-term durations, in license month units, after a main license is procured, to help run fault grading on multiple machines.

The ability of **TurboFault™** to run on networked Linux operating PCs offers a low-cost solution for fault-grading projects.



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