SynTest-Cadence

One-Pass DFT and Synthesis Solution for ASICs

SYNTEST
The Testability Company

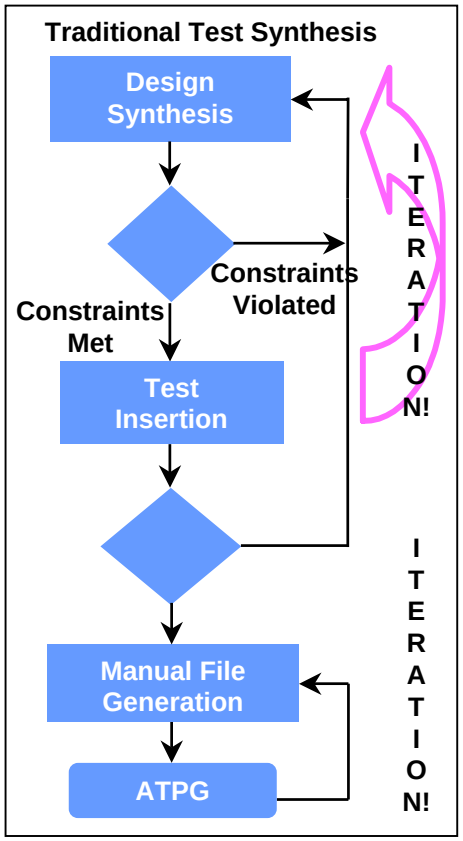
Design-for-Test (DFT) tools and methodologies enable automation of many aspects of the semiconductor testing process, ensuring that the chip comes through tape-out and manufacturing on time, according to specifications and of good quality. DFT tools enable creation of efficient test patterns that detect most major manufacturing defects.

The most prevalent DFT methodology to attain high fault coverage comprises of scan insertion and Automatic Test Pattern Generation (ATPG).

In the traditional test synthesis method, scan chains are inserted after logic synthesis. This results in an iterative process involving scan placement, to ensure that all constraints related to layout and timing closure are properly complied with. The end effect being that this could result in a significant delay to the overall chip design project.

BENEFITS

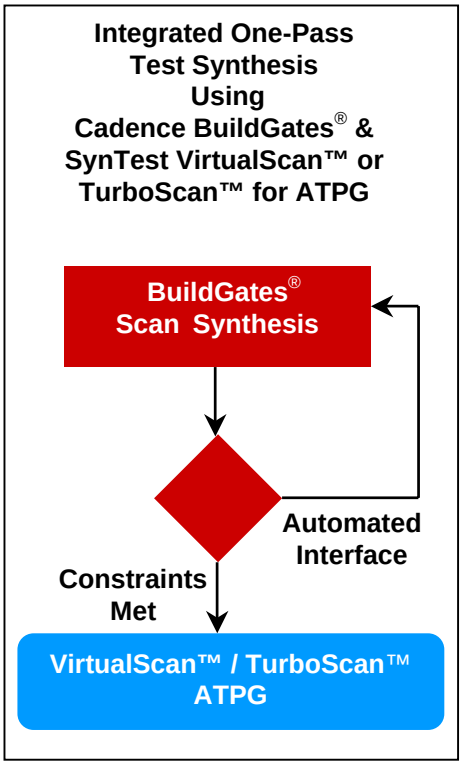
- **Automated, clean and portable design flow.**
- **Concurrent logic and scan synthesis in BuildGates®**
- **Easy-to-use, single command interface "write_atpg_info-syntest" to SynTest's ATPG tools – VirtualScan or TurboScan**
- **Re-stitching of scan-chains based on placement information in .def file from Silicon Ensemble PKS**
- **Rapid efficient test vectors from – VirtualScan or TurboScan**



Focusing on scan insertion, and optimization, to ease the ATPG process, SynTest and Cadence have partnered to provide an automated interface that ensures that layout and timing constraints are met without having to resort to an iterative process.

The Cadence's synthesis tool, BuildGates®, has a full-featured one-pass scan insertion and optimization engine built into it.

It provides an easy, single-command interface "write_atpg_info –syntest" to SynTest's ATPG tools VirtualScan™ or TurboScan™.



VirtualScan provides XtremeCompact test vectors that significantly reduce the costs and time on the ATE.

One-Pass DFT and Synthesis Solution for ASICs

SynTest's DFT-PRO Plus™, DFT tool set, tightly ties with Cadence's verification, synthesis and layout products to provide customers with a complete 'RTL to GDS II' solution and a smooth product design flow.

DFT-PRO *Plus*™ offers an integrated DFT solution covering scan synthesis and ATPG, memory BIST synthesis and boundary-scan (JTAG) synthesis. The corresponding tools generate RTL blocks that fit seamlessly into an existing synthesis flow.

The block diagram alongside shows the One-Pass DFT and Synthesis Solution for ASICs, that enables Cadence customers who use the BuildGates logic synthesis tool, in conjunction with Cadence's Synthesis Placement and Routing (SP&R) tools, to perform automatic insertion of scan chains, followed by compact, high fault coverage ATPG, in one pass.

The diagram depicts a comprehensive flow for insertion of DFT technology into a typical ASIC design, covering scan/ATPG, memory BIST and boundary-scan synthesis, as well as checking for DFT rule violations at both RTL and gate-level stages of an ASIC design.

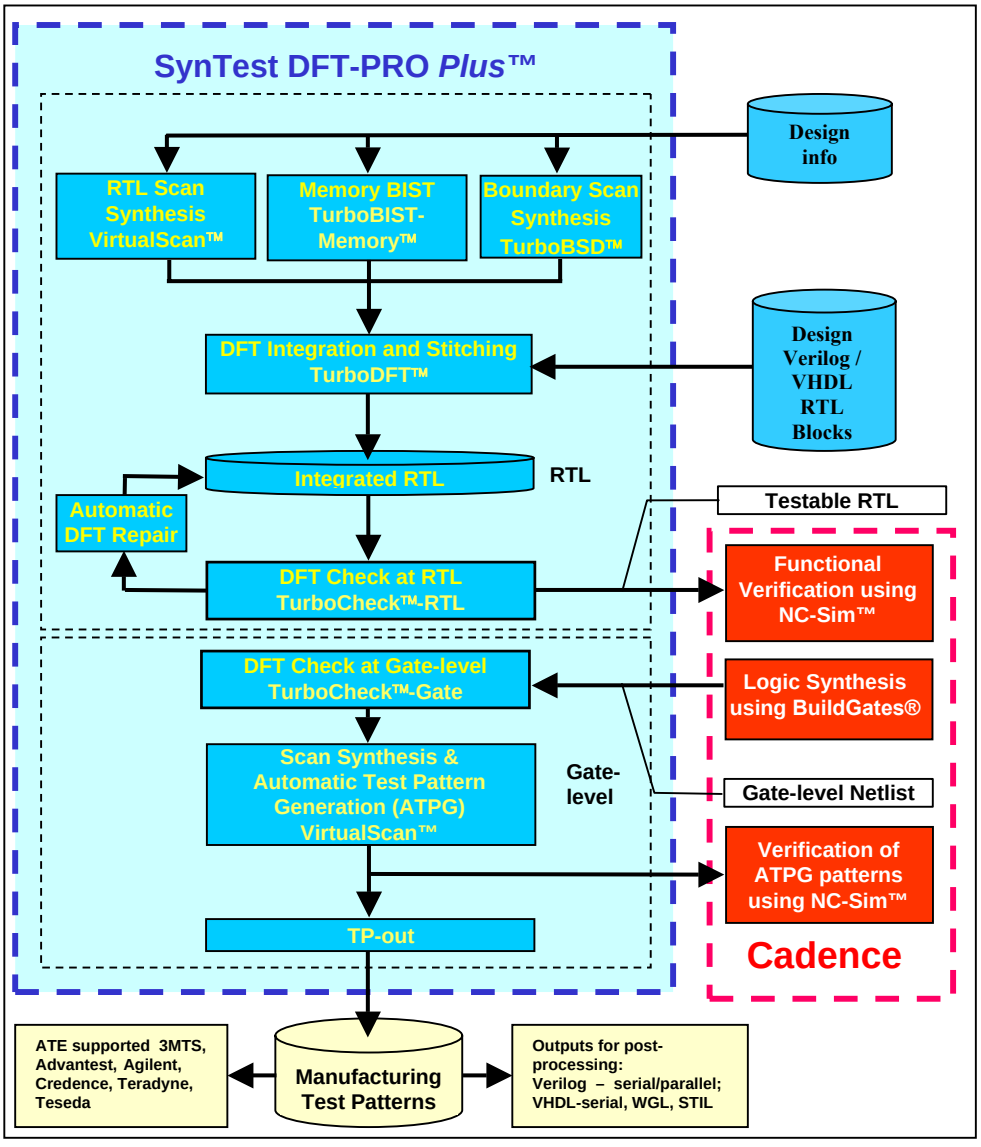
The DFT tools generate DFT blocks at RTL that fit seamlessly into an existing synthesis flow and also ease the design floor planning process.

Further checking DFT violations at RTL averts costly and time consuming post-synthesis surprises.

Individual applications of SynTest and Cadence interfaces are described below.

BENEFITS

- **Improves Quality & Reduces Time and Costs for ASIC Design and Test.**
- **DFT structures at RTL allow designers do quick "what-if" analysis and their impact on area, timing, power, etc., is more predictable.**
- **Check and fix DFT rules violations at RTL to avoid expensive iterations.**
- **Integrates Cadence' NC-Sim™ and BuildGates® with SynTest's DFT-PRO-Plus™, that includes VirtualScan™, to save ATE and test costs.**



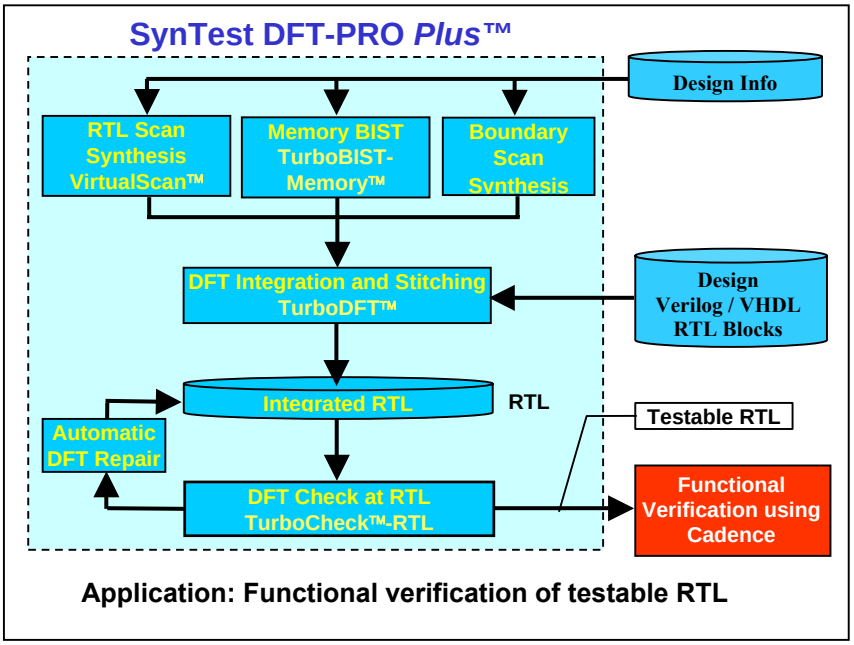
Application:
Functional verification of testable RTL

Cadence Interface: NC-SIM interface, as a part of the Incisive design platform.

SynTest Interface: TurboCheck-RTL

The DFT blocks generated at RTL by the various SynTest DFT tools and the design RTL blocks are automatically stitched together by SynTest's TurboDFT to generate an Integrated RTL.

Before being fed as a testable RTL, via the Cadence NC-SIM interface to its Incisive design platform, for functional verification, the Integrated RTL is fed to SynTest's TurboCheck-RTL to check for DFT rule violations.



Application: Functional verification of testable RTL

Designers can very quickly identify testability problems at the earliest stages of the design cycle, even before the often time-consuming logic synthesis process. TurboCheck-RTL can also be used to identify design coding errors and synthesis constraint violations. TurboCheck tools find many testability problems quickly and automatically, including floating nets, busses and ports, combinational feedback loops, uncontrollable or unobservable nodes, potential bus contention, combinationally gated clocks, and sequentially generated/gated clocks and asynchronous set/reset conditions.

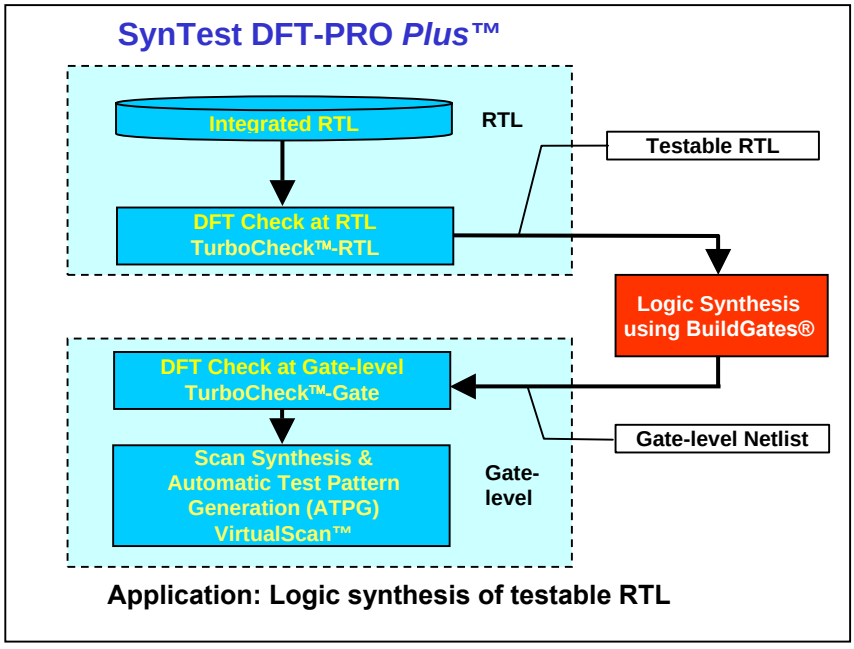
Application:
Logic synthesis of testable RTL

Cadence Interface: BuildGates

SynTest Interface: TurboCheck-RTL and TurboCheck-Gate

The testable RTL is fed to BuildGates for logic synthesis. BuildGates generates a gate-level netlist that is used for scan synthesis and ATPG. Outputs from BuildGates are also fed to other Cadence tools for Placement and routing.

Designers can perform a structural level check on the final synthesized design, using TurboCheck-Gate, to further identify and zero-in on any final testability violations that could not be detected at the RTL level.



Application: Logic synthesis of testable RTL

TurboCheck tools compute and report controllability and observability values according to the structure of the design and identify most common - and not so common - testability issues that could prevent efficient ATPG and fault simulation. TurboCheck also offers automatic insertion of test points using any external scan selection algorithm and analyses the effect of the selection on the testability of the circuit. TurboCheck tools find many testability problems quickly and automatically, including floating nets, busses and ports, combinational feedback loops, uncontrollable or unobservable nodes, potential bus contention, combinationally gated clocks, and sequentially generated/gated clocks and asynchronous set/reset conditions.

Application:
Functional verification of ATPG patterns

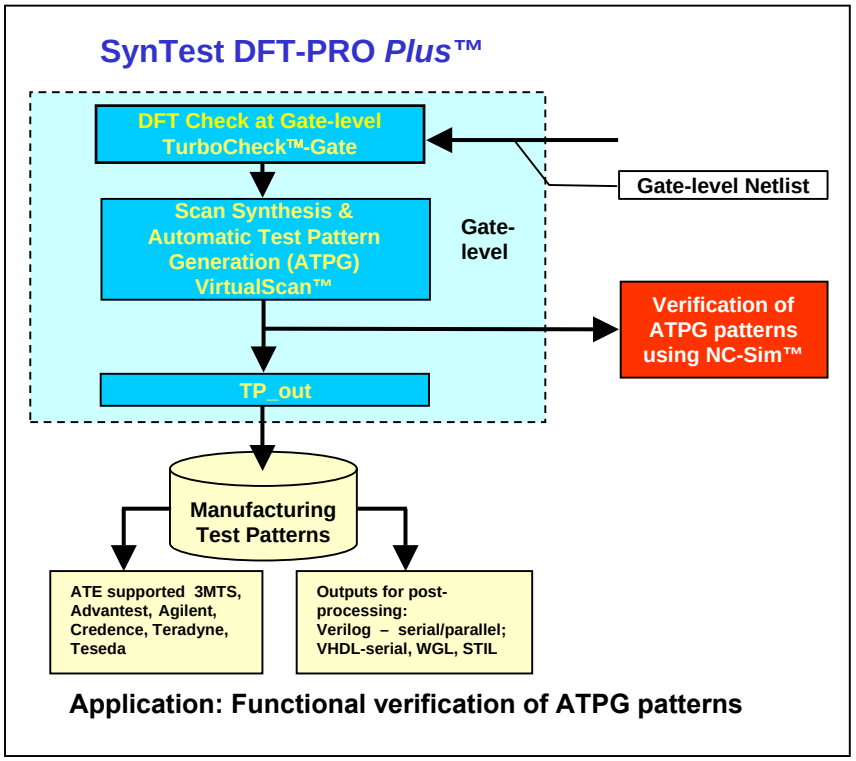
Cadence Interface: NC-SIM interface, as a part of the Incisive design platform.

SynTest Interface: VirtualScan

VirtualScan™, is a tool for scan insertion and compressed ATPG with VirtualScan capability to generate XtremeCompact scan test patterns. This reduces the cost of semiconductor testing by a factor of 5x to 50x through reduced test data volume, test run time and ATE reloads.

These ATPG test patterns are fed via the Cadence NC-SIM interface to its Incisive design platform, for functional verification.

They are also fed via TP_out, as manufacturing test patterns and are available in a variety of formats.



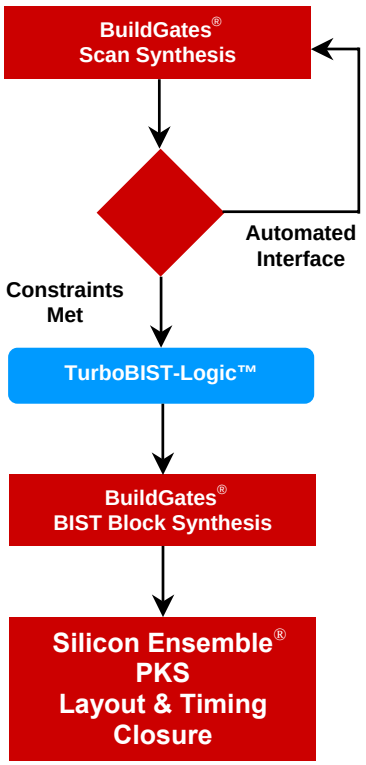
Application: Functional verification of ATPG patterns

Application:
Physical synthesis and integration of Logic-BIST blocks

Cadence Interface: BuildGates or PKS

SynTest Interface: TurboBIST-Logic

BuildGates provides a gate-level netlist. Based on it, TurboBIST-Logic generates logic BIST blocks consisting of the appropriate number of Psuedo-Random Pattern generators (PRPGs), Multiple-Input-Signature-Registers (MISRs) and BIST-controllers. These are fed to BuildGates or PKS for BIST block synthesis, and subsequently to Silicon Ensemble for place and route.



Application: Physical synthesis and integration of Logic-BIST blocks