

# TurboDFT™

## DFT INTEGRATION TOOL SUITE



The Testability Company

### BENEFITS

- Automatically integrate and stitch any combination of DFT cores, such as Scan cores, Memory BIST cores, Logic BIST cores, Analog BIST cores, IP cores, and the Boundary-scan (JTAG) core
- Automatically generate top-level test benches for Memory and Logic BIST cores with or without boundary-scan control
- Assist users in stitching DFT cores into their very deep hierarchical designs
- Eliminate the tedious, error-prone manual stitching process
- Input design can be RTL, Gate-level, or Mixed-level

### PRODUCT DESCRIPTION

TurboDFT™ contains a suite of very useful and powerful DFT integration tools. TurboDFT™ allows users to automatically integrate and stitch DFT cores, whether they are created using DFT tools from SynTest or other vendors. Rtlmsdb scripts and commands are provided for allowing users to automatically stitch DFT cores with or without boundary-scan control. Thus, TurboDFT™ brings “Ease of integration” benefit and eliminates the tedious, error-prone manual stitching process.

Besides the above function, TurboDFT™ can assist users in creating top-level test benches for testing Memory and Logic BIST cores. Users can use the generated test benches to verify each BIST core that may be embedded deep in a hierarchical design.

TurboDFT™ works with SynTest scan (TurboScan™), boundary-scan (TurboBSD™), memory BIST (TurboBIST-Memory™), and logic BIST (TurboBIST-Logic™) products to implement SoC level testability schemes enabling comprehensive board/system level tests.

### PLATFORMS

TurboDFT™ runs on SUN Solaris, HP-UX and Linux platforms, and supports both Verilog and VHDL, either in RTL, gate-level, or mixed-level.

### OTHER INFORMATION

To further reduce silicon debug and diagnosis time, TurboDFT™ test benches can be fed into SynTest’s TurboDebug-SoC™, a low-cost SoC-level DFT prototype debugger.

