

TurboBIST - Memory™

Tools for Embedded Memories

The TurboBIST-Memory family of products from SynTest Technologies, Inc., includes tools for adding highly efficient BIST structures to all types of embedded memories, including SRAMs and ROMs. These tools, part of SynTest's complete suite of solutions for testability analysis, scan ATPG with compression, Logic BIST, and fault simulation, automatically synthesize the BIST logic surrounding the memory blocks and generate the test patterns needed to provide very high fault coverage testing of embedded memories in complex System-on-Chip ICs. A single IEEE 1149.1 compliant TAP controller on the chip can be used to control multiple "BISTed" embedded memory modules of all types, as well as to control scan and Boundary-Scan functions, thus keeping silicon overhead to the absolute minimum.

BENEFITS

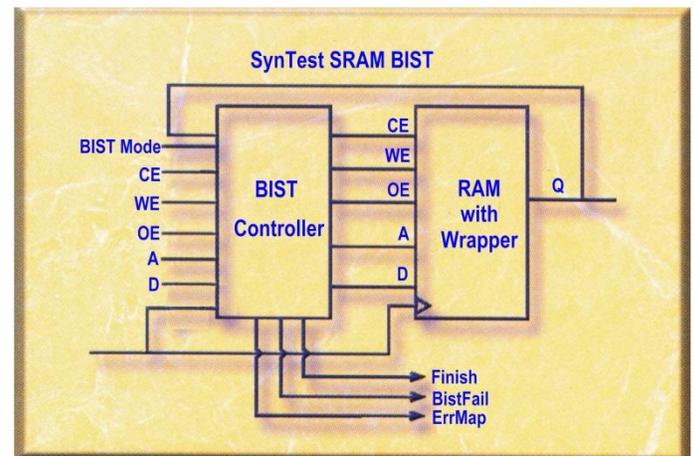
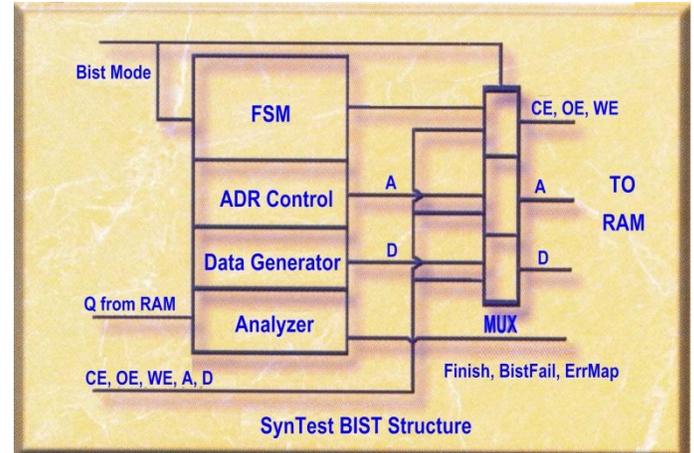
- Handles single-port, two-port, dual-port, or multiple-port SRAM, either synchronous or asynchronous
- Generates Verilog/VHDL test-bench code automatically to reduce test design time
- Outputs Verilog/VHDL Synthesizable RTL Code for Integration into SoC (with synthesis & STA scripts)
- Inserts Comparator at flexible location – inside BIST controller or inside Memory wrapper with pass/fail report after a test session
- Pass/fail signal can be made part of a scan chain
- Reports failed address and/or bits at each cycle when in the diagnosis mode
- Allows users to debug & locate failed RAMs, one at a time
- Automatically adds bypass-multiplexers at memory Q outputs for full-scan test
- Accepts scrambled addresses and data bits
- Uses a small controller size
- Offers Self Diagnosis and Repair features through a companion product, TurboDiagnosis™
- Reports whether SRAM under test is repairable or not.
- Automatically stitches all memory instances together using a companion product, TurboDFT.
- Tightly links with Boundary-Scan product, TurboBSD.

FEATURES

- 100% fault coverage SRAM/ROM BIST synthesis
- Automatic pattern generation for BIST algorithms e.g. March C- (10N), Moving Inversion (13N), March C+ (14N), Checkerboard (5N), Walking Pattern, SOAF
- One shared controller handles different type/sizes of memories
- Allows memories to be tested in mixed serial/parallel mode for power related considerations
- Solutions for high speed memory BIST
- Automatic handling of isolation ring/collar based on configuration information
- Accepts user-specified test algorithm, e.g., 27N
- Retention test support



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Faults Detected using Moving Inversion (MOVI)

Stuck-at faults (SAF), Address decoder faults (AF), Transition faults (TF), Stuck-open faults (SOF), Coupling faults (CFin : Inversion, CFid : Idempotent).

Functional

Test

This test is conducted to ensure that no memory bit is disturbed by a read/write operation on another unrelated memory bit. Each write-operation is preceded and followed by a read operation. MOVI then detects all AFs, followed by all TFs. Unlinked CFins as well as most unlinked CFids are detected. CFids linked with CFins are detected also.

AC Parametric TEST

This test determines the best and worst access times together with address changes. It detects the delay in the address decoder and in the real logic.

BIST for ROM Features

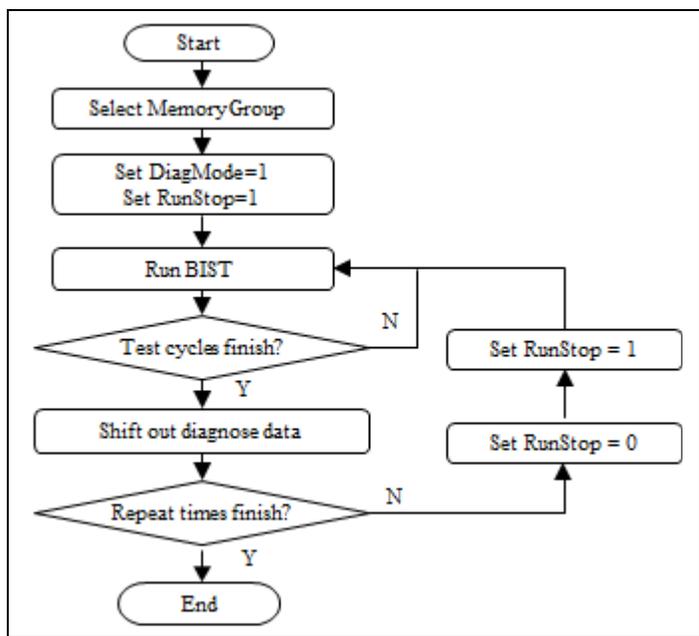
1. Pre-calculates golden signature for the ROM content
2. Synthesizes ROM BIST controller with MISR to compress embedded ROM content into a signature
3. Compares the signature with golden signature to detect defective content
 - a. with embedded golden signature and comparator, or
 - b. by shifting signature out for external comparison

Memory BIST Diagnostics Flow

SynTest TurboDiagnosis-Memory™ product uses the diagnosis information generated by TurboBIST-Memory (as an option).

Platforms

TurboBIST-Memory™ runs on Linux



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MBIST Repair

A companion feature, available as an option, performs automatic diagnosis and repair by supporting One-Time-Programmable (OTP) eFuse interfaces that is common in very deep sub-micron devices.

- Adds ports/data registers in the MBIST memory wrappers for Redundant Row/Col. Control of target memories
- Generates synthesizable RTL for the "eFuse Manager" block. The eFuse Manager is to read back eFuse content into data registers and shift to corresponding redundant column/row control locations of each memory instance during Power-On Reset (POR).
- Integrates the eFuse Manager into designs
- Generates synthesis & timing scripts for the eFuse Manager
- Generates top-level testbenches/vectors to simulate eFuse Manager operation
- Analyzes diagnosis data and stores in a Diagnosis-Results file for future repair references. These Diagnosis-Results can also be used for laser repair.
- Generates C code function(s) to analyze the diagnosis result for on-the-fly eFuse programming (e.g. via top-level or JTAG). The C code is to be integrated into ATE test program.
- Integrates all mentioned programs into ATE test program.
- Generates top-level testbenches/vectors to simulate the eFuse operation.

For the laser-repair fuses, users can still use memory BIST diagnosis analysis results.

Programmable BIST

A companion feature, available as an option, performs the memory test with flexible algorithm controlled from outside. It

- Can be used together with hardwired algorithm
- Generates the instructions automatically
- Generates testbench automatically for the verification
- Supports disturb write/read test
- Can use JTAG interface to control the algorithm
- Allows user defined pattern for the algorithm
- Supports diagnosis flow

MBIST Services

SRAM and ROM BIST can be implemented either by using SynTest's services group or by acquiring licenses for the tools for in-house use. All advanced SRAM BIST features, such as programmable BIST algorithms, are available as a service from SynTest's Applications Engineering group.

Patents

SynTest products are protected by

U.S. Patents: 6,954,887; 6,957,403; 7,007,213; 7,032,148; 7,058,869; 7,124,342; 7,191,373; 7,210,082; 7,228,479; 7,231,570; 7,260,756; 7,284,175; 7,331,032; 7,412,637; 7,412,672; 7,434,126; 7,444,567; 7,451,371; 7,512,851; 7,552,373; 7,590,905; 7,721,172; 7,721,173; 7,735,049; 7,747,920; 7,779,322; 7,779,323; 7,783,940; 7,904,773; 7,904,857; 7,925,947; 7,945,830; 7,945,833; 7,996,741; 8,091,002; 8,161,441; 8,219,945.

European Patents (Registered in the United Kingdom, France, and Germany): 1,360,513; 1,364,436; 1,370,880; 1,377,981.

Japan Patents: 4301813; 4733191; 4903365.

China Patent: ZL02804862.1.

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