

TurboScan™

TOOL SET FOR SCAN SYNTHESIS AND ATPG

Today, integrated chips with multi-million gates, containing logic, memory and analog functions are becoming commonplace. At the same time, meeting tight time-to-market schedules, controlling costs and maintaining high quality standards are critical to the success of any such new development.

Design-for-Test (DFT) tools and methodologies enable automation of many aspects of the structural testing process, ensuring that the chip comes through tape-out and manufacturing on time, and of proper quality. DFT tools enable creation of efficient test patterns that detect most major manufacturing defects. Effective DFT methodologies available today for structural testing include scan synthesis and ATPG (Automatic Test Pattern Generation), logic BIST (Built-in Self-Test) and fault simulation.

TurboScan™ is an advanced full-scan test suite. It includes a scan synthesizer and an Automatic Test Pattern Generator. The scan synthesizer supports full scan methodologies. The ATPG engine uses advanced search and compaction algorithms to produce very high fault coverage test patterns with very concise pattern sizes.

The TurboScan ATPG algorithms also work on asynchronous sequential circuits containing gated clocks, RAMs, ROMs, tri-state gates, asynchronous set/reset functions, and unidirectional transistors. It detects static and timing related defects.

TurboScan uses an advanced 64-value search algorithm. This reduces the ATPG search space, especially for circuits containing non-scan flip-flops or other uncontrollable signal sources, and thereby improves the speed of the ATPG process and the circuit's fault coverage.

SynTest's patent-pending multiple-capture-per-cycle scheme for ATPG significantly reduces the total test time of designs with multiple-frequency clock domains, as only one scan-in/scan-out phase is deployed for each pattern.

Proprietary static and dynamic compaction algorithms are used to generate very compact ATPG patterns. These help reduce ATE test costs, by reducing the test time and avoiding reloading of patterns.

TurboScan generates patterns for commonly used fault models e.g. Stuck-at, Transition Delay, Bridging, Path Delay, etc. The transition delay fault model needs an extra capture clock edge to detect a signal slow-to-rise or slow-to-fall. So there are two captures within the capture window. It is often called double-capture. The first capture clock launches a transition, and then at the second capture clock edge, the scan chain captures the delay effect. The time between the first and the second capture clock edge can test the at-speed effect of the device. An extended feature is test patterns for the path-delay faults of user given set of path(s). A path-delay fault is defined as a path (from a flip-flop output to a flip-flop input) being slow to rise or fall. Normally, users derive those paths, which are timing critical paths, from a static timing analysis tool.

When power is a concern, ATPG also generates patterns for low power devices with minimal toggles during shift operation as well as minimal power in capture cycles.



SYNTEST

The Testability Company

BENEFITS OF TURBOSCAN

- Improved design quality through very high fault coverage test patterns
- Generates Stuck-at, transition, bridging fault, Iddq, path-delay patterns
- Reduced test costs - shorter test times and reduced test data volumes
- Easy to integrate into existing design flow
- ATPG patterns can also be generated for designs that have scan chains inserted using other vendor's scan synthesis tools.
- Minimum Silicon Usage/Overhead
- Short CPU Times

FEATURES

- Combinational ATPG
- Contains cycle-based good and fault simulation engines for fault detection.
- Stuck-at, transition, bridging fault, Iddq, path-delay patterns
- Multi-Capture for reduced test pattern and power
- Patented At-Speed capture scheme
- Multi-Cycle-Path Support
- Multi-Detection (N-Detect) for higher test quality
- Low power support by minimal toggle
- Static & Dynamic test compaction for test pattern reduction
- Smart-Capture for ATPG time reduction.
- Post-ATE diagnosis capabilities
- Generates patterns and calculates fault coverage for IDDQ faults
- Uses 64-value search algorithm to improve speed and fault coverage
- Scan Synthesis and Debug
 - Automatic repair of testability rule violations
 - Scan cell insertion
 - Scan chain synthesis based on clock domains
 - Scan chain extraction support in case of already-scanned netlist
 - Scan chain debug utilities
- Flexible transparent/non-transparent latch options
 - No overhead, no potential timing violations, no potential feedback loops, clock fault detection
- Non-scan positive/negative flip-flops
 - Can propagate values from D/S/R to Q
 - Fewer undetectable faults (including clock faults)
- Multiple internal/external clocks
 - Allows clock delays among clocks and can generate patterns within one clock cycle
- Smart tri-state bus handling
 - Contention free behavior before and after capture
 - No need to run fault simulation after ATPG to drop patterns
- Sophisticated Multiple and Multi-port RAM support
 - Black box, bypass and wrapper modes
- Advanced compaction algorithm
 - Static and dynamic compaction
 - Typical more compact pattern sizes - reduce test costs
- ATPG outputs for post-processing are available in:
 - Standard formats: Verilog Serial/Parallel, WGL, or STIL
 - For specific ATE testers, such as Advantest, Agilent, Credence, Teradyne, or Teseda

TurboCheck-Gate™ (Companion product):

It analyzes a gate-level design with or without scan, for DFT testability. It calculates the controllability and observability for designs assuming non-scan, partial-scan or full-scan implementation. It uses a set of rules to identify and report problems that may cause low fault coverage.

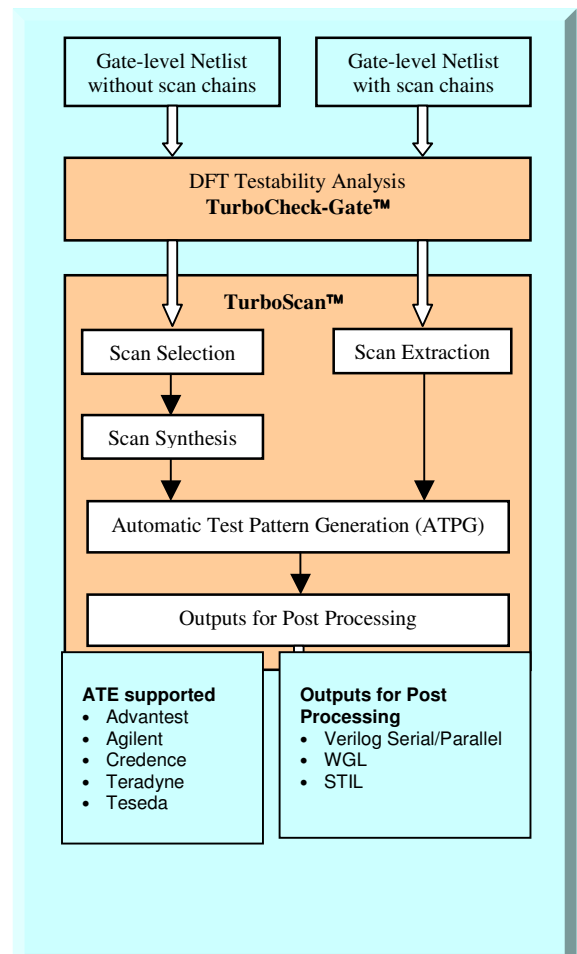
DESIGN FLOW

A gate-level netlist is first run through TurboCheck-Gate to check for DFT violations. It is then fed to TurboScan where scan selection and synthesis is performed. The scan-inserted netlist is then fed to the ATPG for test pattern generation. The test patterns can be output in a number of different formats for post processing and use on Automatic Test Equipment (ATE).

TurboScan can also work with gate-level netlists that have scan chains already inserted into them by other commercially available scan synthesis tools.

In this case also the gate-level netlist is first checked for DFT violations, using TurboCheck-Gate. Then scan extraction is performed to obtain relevant scan information.

The scan-inserted netlist is then fed to the ATPG for test pattern generation, as mentioned above.



SCAN TEST FOR MULTIPLE-CAPTURE-PER-CYCLE SCHEME

SynTest’s multiple-capture-per-cycle scheme for Automatic Test Pattern Generation slashes the total test time of designs with multiple-frequency clock domains, as only one scan-in/scan-out phase is deployed for each pattern.

Figure 1 shows a simple circuit with only one scan chain and the basics of scan test for a single-frequency design. Here, the total test time for scan testing depends on the amount of time needed for each scan pattern test and on the total number of scan test patterns.

This can be extended to a multiple-frequency design by identifying scan flip-flops in each clock frequency domain and forming a scan chain or multiple scan chains for each frequency (Fig. 2). In the normal operational mode of a chip, many of these clock domains mutually interact, and this can occur at different asynchronous moments (called interclock-domain activity). Such "external" clock-domain interaction can result in instabilities, and thus invalidate the capture-cycle results. As is well documented, ATPG schemes based on combinational logic handling will not be able to handle such interactions. Consequently, a hold mode or isolation circuit typically is employed in such schemes to protect the accuracy of results during the capture cycle of each scan chain.

In this case, scan pattern values are scanned in for all chains, but only one clock domain, called the “One-hot clock” with one scan chain is used in the testing, during the capture cycle. The process starts with one frequency domain, and all other clock domains are placed in a hold, or inactive, mode. The results are scanned out and the process is repeated for the rest of the clock domains. As can be seen, the test time needed for each pattern equals the number of clock domains multiplied by the time for each pattern to scan in, go through capture and scan out. This result then is multiplied by the number of patterns for the full scan test.

SynTest’s multiple-capture-per-cycle scheme is shown in Figure 3. Scan pattern values are scanned in for all scan chains, a multiple-capture-per-cycle follows and the final results are scanned out. The resulting total test time for each scan pattern is given by the time for each pattern to scan-in, its additional time to the multiple-capture interval and the time needed to scan out. Note that the multiple-capture-per-cycle takes a little longer than the capture cycle for schemes based on one-hot clock, but is much shorter than time taken by the scan-in and scan-out operations. Thus, the test compaction factor equals the total number of clock domains.

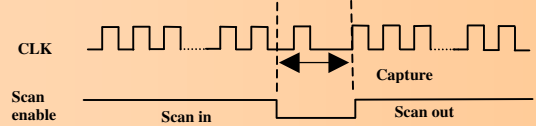


Fig. 1 – Time required on a tester to process a single scan chain

Test time $[t_{sc}] = [t_{sin}] + [t_{cap}] + [t_{sout}]$
 Where: t_{sc} = time required to process a single scan
 t_{sin} = time required to input (load) a scan chain
 t_{cap} = time required for a capture-cycle
 t_{sout} = time required to output (unload) a scan chain

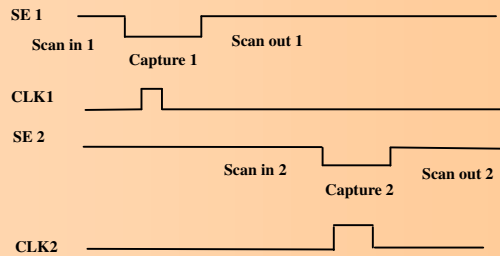


Fig. 2 – Time required on a tester to process multiple scan chains, assuming all scan chains are of the same length

Total test time $[t_{tot}] = [n_{sc}] * [t_{sc}] = [n_{sc}] * [t_{sin} + t_{cap} + t_{sout}]$
 Where: n_{sc} = number of scan chains being processed

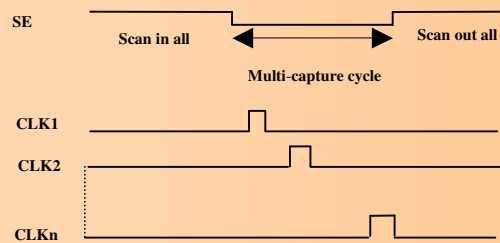


Fig. 3 – Time required on a tester to process multiple scan chains using SynTest’s proprietary “multiple-capture-per-cycle” methodology

Total test time $[t_{syn-tot}] = [t_{sin}] + [n_{sc}] * [t_{mcap}] + [t_{sout}]$
 Where: t_{mcap} = time required for a multi-capture-cycle

Since $[t_{sin}]$ or $[t_{sout}]$ are $\gg [t_{cap}]$; and $[t_{mcap}] \sim [t_{cap}]$ the test time required to process multiple scan chains using SynTest’s proprietary “multiple-capture-per-cycle” methodology is only $1/[n_{sc}]$, the time required for conventional processing. Thus, the saving in test time using multi-capture-per-cycle is $[n_{sc}]$.

OTHER PRODUCTS FROM SYNTEST

VirtualScan™ is SynTest's solution to combat a surge in test data volume and test cycle volume. Up to 50x compaction is achievable with VirtualScan™. An extremely large number of short scan chains within the SOC can be virtually accessed from outside the chip with a limited number of pins assigned as scan pins. SynTest's patent-pending circuitry is used to broadcast each external scan-input chain to a user-selectable number of internal scan chains and then compact results into the original external scan-output chains.

UltraScan™ is SynTest's solution to reduce test time 50x to 500x. It is used along with VirtualScan™ to reduce the overall test cost. UltraScan™ extends life of existing ATE for testing large SOC designs. With UltraScan™ a small number of high-speed I/O pads are adequate to run a scan ATPG test for a design with a large number of internal scan chains of shorter length. It achieves pin reduction through proprietary TDDM/ TDM circuitry. Overall shorter test load times are realized by taking advantage of the unutilized bandwidth available on high-speed channels on the ATE during low-speed scan-shift operation.

TurboBIST-Logic™: A tool suite for logic BIST; it helps reduce ATE tester costs during production, by using Built-In Self Test methodology. It is ideal when dealing with SOC designs with multi-million gates/primitives, multiple clock domains and multiple and high frequencies. It detects timing faults by using "at-speed" testing - a patented capture scheme. It helps reduce test preparation time and test costs when using multiple instantiation of "legacy" logic circuit blocks or re-using IP cores in different designs. It is ideal for in-field remote testing or non-invasive testing, prototype debug/diagnosis and for the wafer sorting process.

TurboBIST-Memory™: A memory BIST tool for embedded memories including SRAM and ROM. It enables simultaneous multiple BIST memory tests via a shared controller. It outputs synthesizable RTL BIST controllers and logic synthesis scripts. It also generates a Verilog test bench automatically.

TurboBSD™: A boundary-scan test suite, it performs IEEE 1149.1 compliant boundary scan logic synthesis, generates boundary scan description language (BSDL) files and boundary scan test patterns, including verification and parametric test benches. It also generates RTL & Gate-level netlists in Verilog.

TurboCheck™: RTL and gate-level DFT testability analysis tools. At RTL it identifies testability problems at the earliest stage of the design cycle, even before synthesis, preventing costly and time-consuming iterations in the design process. At gate-level, it analyzes designs with or without scan, for DFT testability. It uses a set of rules to identify and report problems that cause low fault coverage. Both offer optional repair capability.

TurboDFT™: A tool for DFT integration and stitching, it eliminates the tedious, error-prone manual stitching process by automatically integrating and stitching any combination of DFT cores, such as scan cores, memory BIST cores, logic BIST cores, analog BIST cores, IP cores, and the boundary-scan (JTAG) core.



Corporate Headquarters:
SynTest Technologies, Inc.
505 South Pastoria Avenue, Suite 101,
Sunnyvale, CA 94086, USA
Offices and distributors worldwide –
Please call, e-mail or visit our web site for the one closest to you. <http://www.syntest.com>

ORDERING INFORMATION

TurboScan™, VirtualScan™, UltraScan™: For Scan Synthesis and ATPG for stuck-at faults. Plus select test program format for one ATE.

Options:

TurboScan-TR™: For transition faults ATPG.

TurboScan-PD™: For path delay ATPG.

TurboScan-BF™: For bridging faults ATPG.

TurboScan-LP™: For low power ATPG.

Other Products from SynTest

• **TurboBSD™**: For Boundary-scan Synthesis

• **TurboBIST-Memory™**: For Memory-BIST Synthesis

• **TurboDFT™**: For DFT Integration

• **TurboCheck™**: For DFT Rule Checking

• **DFT-PRO™**: A comprehensive package of DFT tools which includes TurboScan™, TurboBSD™, TurboBIST-Memory™, TurboDFT™: and TurboCheck™:

• **TurboBIST-Logic/Memory™**: BIST Tool Suite

• **TurboFault™**: For Concurrent Fault Simulation

• **TurboDiagnosis™**: For scan chains diagnosis

PLATFORMS

TurboScan™ runs on Sun Solaris, HP-UX and networked Linux operating PCs.

OTHER PRODUCTS FROM SYNTEST

TurboFault™: A concurrent fault simulator useful where scan/ATPG technology cannot be used or to enhance fault coverage attained with scan/ATPG technology. It is the fastest high capacity concurrent fault simulator based on the proprietary algorithms in fault simulation technology. With its low memory consumption, user- definable fault detection criteria, fault-tracing, back-tracing and crash recovery capabilities, it combines high performance with versatility and accuracy. It accepts fault lists from most ATPG tools. As input stimuli, it can handle VCD, WGL and Novas FSDB.

SynTest is now offering Solutions For Diagnosis and Failure Analysis of Scan Chains and Logic BIST with a set of products. The products offered are –

TurboDiagnosis-Scan™, TurboDiagnosis-VScan™, TurboDiagnosis-LogicBIST™.