TurboBIST-Logic™

Logic BIST Tool Suite

The Testability Company

Today's SOCs (System-on-Chip) can contain hundreds of memories, several types of logic, dozens of functional blocks obtained from diverse sources, and multiple clocks operating at multiple frequencies. This brings in its wake problems of defining a proper test strategy, optimizing test costs and the time required for testing. External access, embedded self-tests and diagnostics go a long way towards helping solve the test challenge.

It is in this environment that Logic BIST (Built-In Self-Test) makes itself a valuable ally, if not an indispensable tool. One of Logic BIST's greatest virtues is its ability to test a circuit at its full operating speed. Something that even some very expensive external automated test equipment (ATE) systems cannot do.

Further, "at-speed" testing, as it is called, has become essential for submicron chips, in which path delays and other timing faults have become crucial to their operation. Only true clock-rate testing can discover these. Thus, Logic BIST goes beyond the familiar stuck-at fault model and has become essential if timing faults are to be included in the coverage.

The TurboBIST-Logic™ is a powerful, yet easy-to-use, package to create Logic BIST circuits for embedded cores or IPs. It is suitable for IP-based SOC designs to reduce the cost of manufacture tests and improve the quality by using "at-speed" testing.

It generates BIST architecture for single clock, multiple clock and multiple frequency domains. In these cases the "at-speed" strategy is used in TurboBIST-Logic™. The "at-speed" operation features a proprietary (patent-pending) multi-capture scheme which allows the core to be tested using "true" clocks; and a fault simulator, which supports stuck-at, transition, and path-delay (upcoming) fault models. Other patent-pending features help implementation of the Logic BIST without adding to the timing closure burden in the back-end layout phase.

TurboBIST-Logic™ allows users to use a number of strategies for improving fault coverage, such as increasing the number of BIST patterns, re-seeding, adding Test Points, or Top-up ATPG using SynTest's proprietary sequential ATPG technology that supports full-scan and partial-scan (TurboScan™-ATPG).

TurboBIST-Logic™ generates synthesizable RTL blocks as well as script files, which can be used with tools from leading EDA vendors for logic simulation, synthesis and static timing analysis (STA).

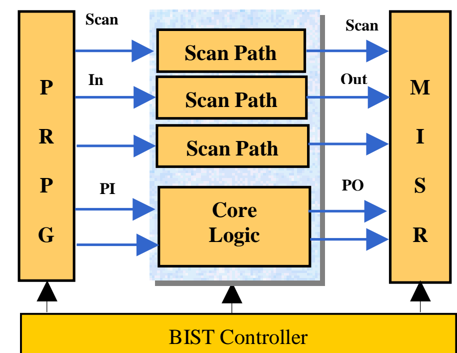
TurboBIST-Logic™ also works with SynTest's boundary-scan synthesis tool, TurboBSD™ to implement SOC level testability schemes, enabling comprehensive board / system level tests.

Methodology

TurboBIST-Logic™ is based on the scan method as the fundamental DFT technology. The stimuli originate from a Pseudo-Random Pattern Generator (PRPG) and the test responses are compacted into a Multiple-Input Signature Register (MISR), as shown in the diagram. In case of multiple clock-domain multi-frequency circuits, a pair of PRPG and MISR can be used for each individual clock domain or frequency, along with its corresponding BIST controller.

Benefits Of Logic BIST

- Helps reduce ATE tester costs during production, by using "at-speed' testing. Ideal when dealing with SOC designs with multi-million gates/primitives, multiple clock domains and multiple frequencies and high frequencies.
- Helps improve quality of sub-micron chips, by detecting path delay and other timing faults by using "at-speed' testing and a patent-pending capture scheme.
- Offers comprehensive fault detection when testing circuits with multiple clocks and multiple frequencies using SynTest's patent-pending capture scheme for true multi-clock multi-frequency handling.
- Helps reduce design time and test costs as well as ensures higher quality and reliability when using multiple instantiation of "legacy" logic circuit blocks or re-using IP cores in different designs.
- Can help in the wafer sorting process and thereby help reduce packaging costs.
- Ideal for in-field remote testing or non-invasive testing of crucial electronic equipment.
- Helps during prototype debug / diagnosis.



Basic methodology for Logic BIST
PRPG = Pseudo-Random Pattern Generator
MISR = Multiple-Input Signature Register
PI = Primary Input; PO = Primary Output

APPLICATIONS

During Production

- SOC designs with multi-million gates:
  The number of patterns generated using Automatic Test Pattern Generation (ATPG) needed to adequately test multi-million primitive designs tends to be very large and applying these large number of patterns takes a very long time on an Automatic Test Equipment (ATE). This could significantly drive up the total test cost for the chip. "At-Speed" Logic BIST offers an alternative solution, which significantly reduces the time required on the testers, driving the chip test cost down.

- SOC designs with high frequencies:
  The cost of ATE increases significantly when testing at high speeds is a requirement. Also, appropriate ATE may not be available due to scheduling conflicts. Testing high-speed circuit blocks with Logic BIST enables use of low-cost testers to test complex SOCs easing the high-speed ATE scheduling conflicts, and also helping to keep the tester costs down.

- Detecting timing faults:
  For sub-micron chips, path delays and other timing faults become crucial to their operation - especially when clock frequencies are very high. These faults cannot be detected using ATPG test executed at slower speeds. Only "true clock rate" or "at-speed" testing can detect these faults. Logic BIST facilitates such "at-speed" testing and enables detection of transition delay, path delay faults and other timing faults. SynTest offers a patent-pending capture scheme for detecting timing faults.

- SOC designs with multiple clocks and multiple frequencies:
  For testing circuits with multiple clocks and multiple frequencies, operating the logic at the desired "at-speed" frequency allows for cross-clock-domain fault transfers and hence more comprehensive fault detection.
  SynTest offers a patent-pending capture scheme for true multi-clock multi-frequency handling.

- IP cores:
  In large SOC designs, it is becoming common to re-use multiple instantiation of "legacy" logic circuit blocks or use IP cores available from many vendors. Overall test creation as well as test execution time for SOC designs can be considerably reduced by implementing Logic BIST for such blocks/cores and then using such "BISTed" blocks/cores in the design.

  Such BISTed blocks/cores can also be re-used in subsequent designs, again helping to reduce test cost and to ensure higher quality and reliability.

During Wafer Sort

Simple Go/No-Go testing can help in the wafer sorting process and thereby help reduce packaging costs. Similarly such testing can also be used to test the quality of PCBs used in the system.

During Prototype Debug/diagnosis

Scan chains based Logic BIST allows diagnosis analysis of a failing design, pin pointing the pattern where the test fails and then allowing scanning out of the results to identify the failing instance.

In the field

Simple Go/No-Go testing helps in monitoring the functioning / performance of the SOC. External access is easily provided through the Test Access Port (TAP) via boundary scan (JTAG) link. This is ideal for remote testing or non-invasive testing of crucial electronic equipment.

FEATURES

- Scan based system
- Automatic scan and BIST design rule check and repair
- Optimized PRPG and phase shifter design
- Patent-pending capture scheme for “true” multi-clock multi-frequency handling
- Minimal clock manipulation
- Fast fault simulation for stuck-at, transition delay and path delay faults
- Automatic signature generation using multiple inputs (MISR)
- Can handle mixed-edge flip-flops and gated clocks
- Capability of re-timing for design re-targetting for technology or geometry
- Insignificant addition to design iterations related to timing closure
- Low clock glitch risk in shift and low overtest risk
- Synthesizable RTL code generation for PRPG, MISR, and BIST controller.
- Script files generated can be used with tools from leading EDA vendors for logic simulation, synthesis and static timing analysis (STA).
- Flexible PI/PO handling.
- Improve fault coverage through
  - Varying the number of LBIST patterns
  - Re-seeding of PRPG
  - Efficient clock-domain-based test point insertion
  - Top-up ATPG
- Very compact test set generation for top-up ATPG, using SynTest’s TurboScan™-ATPG
- Programmable and flexible diagnostic features
- Advanced scan synthesis features, including scan selection, repair, reordering and debug
- Link for boundary-scan (JTAG) interface
- Debug capabilities available through SynTest’s TurboDebug-SOC/Logic

FLOW

The typical Logic BIST flow as shown in the diagram, starts with a gate-level netlist. As the scan method is the fundamental DFT technology used, the netlist is checked to see whether it has scan inserted into it.

If the netlist has scan already inserted, the first step is to check it for scan design rules. Subsequently, scan extraction is performed.

If there is no scan inserted in the netlist, the first step is to perform scan insertion, which consists of scan selection and scan synthesis and generating a new scanned netlist.

The next step is to configure the Logic BIST, which generates the PRPG, MISR and BIST controller circuits. The user needs to define either the number of PRPG patterns or the desired fault coverage in the BIST structure.

These configurations are then checked for BIST rules violations. Subsequently, fault simulation is run and calculations performed to obtain the circuit's fault coverage and the final MISR signature.

The circuitry used to run fault simulation on the BISTed design is the same as used in SynTest's powerful industry leading fault simulation tool, TurboFault™.

After running fault simulation, if the circuit's fault coverage (F.C.) is too low, a number of strategies are available to improve the fault coverage. Each strategy obviously has an impact on the "total test time", "timing overhead of the design", "area overhead" and "overall improvement in fault coverage". Users need to consider the trade-offs before selecting one or usually a combination of these strategies to suit their overall requirements. These strategies are described separately below.

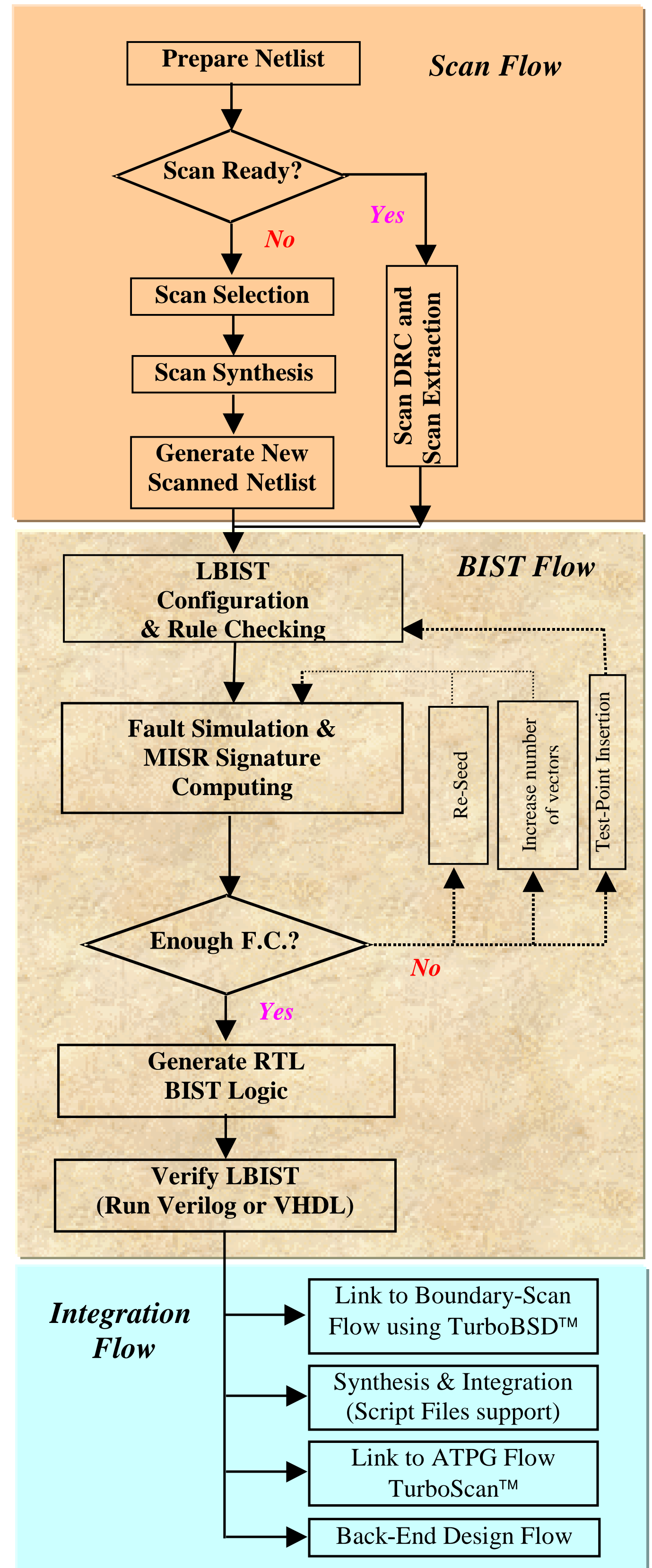
Once the fault coverage reaches a satisfactory number, the Logic BIST RTL is generated along with the script files for integration. Subsequently, a logic simulator is used to simulate the generated BIST RTL test bench in order to verify the BIST operation.

Synthesis and integration

The script files are generated in order to synthesize the design and run the static timing analysis (STA). These script files can be integrated to run the whole chip synthesis and timing check. The script files can be used with tools from leading EDA vendors for logic simulation , synthesis and static timing analysis (STA).

By linking to a boundary-scan flow, via TurboBSD™, you can simply use the TAP controller to drive the LBIST operation. The program generates the serial vector format .svf and guides TurboBSD™ to link the necessary signals to the interface of LBIST.

After integration, you can continue to run the back-end design flow. Whenever the logic function of the netlist is changed, please re-run the flow to update the final expected MISR signature and run "back annotation timing check" to ensure that the timing is safe under the BIST mode.



STRATEGIES FOR IMPROVING FAULT COVERAGE

Each strategy obviously has an impact on the "total test time", "timing overhead of the design", "area overhead" and "overall improvement in fault coverage". Users need to consider the trade-offs before selecting one or a combination of these strategies to suit their overall requirements.

- **Increasing the number of BIST patterns:**
  If you set a pattern number, but it cannot achieve the expected fault coverage, you can increase the number of patterns in the LBIST configuration program and re-run fault simulation.

- **Re-seeding:**
  Multiple seeds can be shifted through the JTAG ports. There is no need for extra hardware and timing overhead. The major benefit is getting higher fault coverage by selecting effective seed numbers. Either the user can select the seed numbers or the tool can select them.

- **Adding Test Points:**
  If the fault coverage is low after fault simulation, TurboBIST-Logic™ can add test points to increase the fault coverage. The test points can be inserted as a separate scan chain, after the scan chains are built. In this case, the circuit needs to be re-scan synthesized with the new scan chain added. Scan extraction also needs to be repeated before a new BIST structure is generated. Due to these additional steps, the iterative process takes a longer time.

- **Top-up ATPG:**
  For increasing the fault coverage to very high percentages and for reducing overhead related to Test Points insertion, TurboBIST-Logic™ works in tandem with SynTest's proprietary sequential ATPG technology that supports full-scan and partial-scan (TurboScan-ATPG). A link is provided in the BIST flow "-link_to_atpg", which will keep the scan chain and test interface for Top-up ATPG. As a result you will be able to run the Top-up ATPG for these faults undetected by the PRPG patterns and increase the overall fault coverage.

  This hybrid methodology overcomes the basic drawback of ATPG requiring a long time, as now only a relatively small number of faults are still to be detected.

Platforms
TurboBIST-Logic™- runs on Sun Solaris, HP-UX and linux operating PCs networked on an UNIX server.

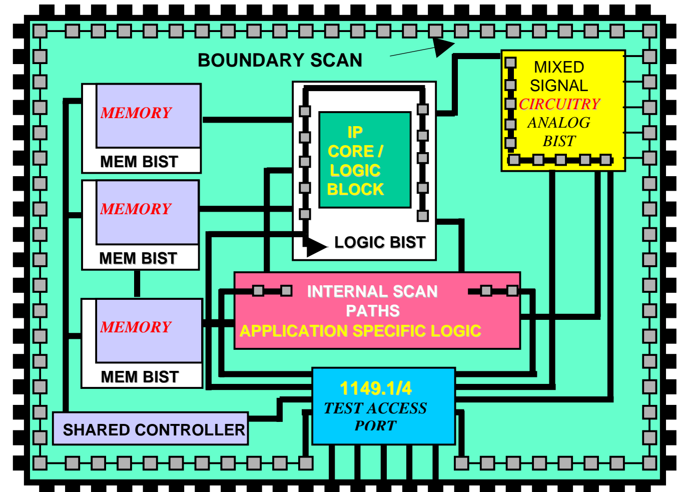
Debugging/Diagnosis

TurboDebug-SOC™/Logic is a product for simulating the Logic BIST circuit and locating faults. It uses the boundary-scan chain to input user-specified vectors in .svf format. It operates on any PC that has a PCI slot and runs on Linux as OS.

LINK TO BOUNDARY-SCAN (JTAG) FLOW

To implement SOC level testability schemes, enabling comprehensive Board / System level tests, TurboBIST-Logic™ also works with SynTest's Boundary-Scan Synthesis tool, TurboBSD™

By linking to TurboBSD™, you can simply use the TAP controller to drive the Logic BIST operation. The program generates the serial vector format .svf and guides TurboBSD™ to link the necessary signals to the interface of TurboBIST-Logic™.



"TRUE CLOCKS"

If a circuit has three clocks, say 150MHz, 100Mhz and 66Mhz, TurboBIST-Logic™ will test the circuit at these three frequencies and not at 150MHz, 75MHz and 37.5MHz using the divide-by-two approach employed by other Logic BIST tools.

ORDERING INFORMATION

- **TurboBIST-Logic™-** Logic BIST Tool Suite

Options

- TurboScan™-ATPG: For Top-up ATPG
- ATE Test Program Outputs
- TurboBSD™: For Boundary-Scan Synthesis
- TurboDebug-SOC™/Logic: For Logic BIST Debugging and Diagnosis

Other Products from SynTest

- TurboBIST-Memory™: For Memory-BIST Synthesis
- TurboDFT™: For DFT Integration
- TurboCheck™: For DFT Rule Checking
- TurboScan™-Synthesis: For Scan Synthesis
- TurboDebug-PCB™: For Debugging Interconnects on PCBs
- TurboFault™: For Concurrent Fault Simulation

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