Booth # 1107

Exhibit Hours
Tuesday, November 8: 10.00 a.m. – 7:00 p.m.
Wednesday, November 9: 9:30 a.m. – 6:00 p.m.
Thursday, November 10: 9:30 a.m. – 1:30 p.m.

ITC is offering free exhibits-only registration to visit the exhibit hall on Wednesday from 1:30 p.m. to 6:00 p.m. and on Thursday from 9:30 a.m. to 1:30 p.m. On-site registration for this special opportunity begins on Wednesday at 1:30 p.m. at the ITC registration area in the Austin Convention Center. (Lunch is not included.)

Tuesday, Nov. 8, 7:00 p.m. – 8:30 p.m.
Panel 5 - The ITC Test Compression Shootout
S. Davidson, Sun Microsystems (Moderator/Organizer)

Test compression has been a hot topic at ITC as researchers have proposed ways to help fit our increasingly large test vector sets into the same amount of ATE memory. What are the pros and cons of each? In this panel seven methods are compared on a real design example.

Panelists: B. Keller, Cadence Design Systems • K. Kim, Intel • J. Rajski, Mentor Graphics, • N. Touba, The University of Texas at Austin • S. Wu, SynTest Technologies

Wednesday, Nov. 9, 11.00 a.m. – 11.30 a.m.(Room 207A/B/C)
ITC Corporate Track - Session “EDA”
Session chair: Rob Aitken

Session C2.2
“SynTest takes scan-test data compression to new levels”
SynTest unveils a RTL tool suite that includes UltraScan(tm) to reduce scan-test time by 100x and introduces its DFT technology for "at-speed testing" as an IP.

Presented by: Nayan Pradhan

Wednesday, Nov. 9, 4:00 p.m. – 6:00 p.m.
SESSION 36 - BIST Pattern Generation
V. Iyengar, IBM (Chair)
K. Hatayama, Renesas Technology (Coordinator)

36.4 UltraScan: Using Time-Division Demultiplexing/Multiplexing (TDDM/TDM) with VirtualScan for Test Cost Reduction
S. Wu, L-T. Wang, K. Abdel-Hafez, B. Sheu, F-S. Hsu, S-H. Lin, M-T. Chang - SynTest Technologies; X. Wen, Kyushu Institute of Technology