

# SynTest Proprietary Technology for At-Speed Testing and Test Compression

Laung-Terng (L.-T.) Wang, Ph.D.

President & CEO

SynTest Technologies, Inc.

May 13, 2008

# Outline

- Company Background
- At-Speed Scan/BIST Patents
  - Staggered Double-Capture
  - Staggered Skewed-Load
- Test Compression Patent - VirtualScan
- Test Compression Patent - UltraScan
- Conclusions

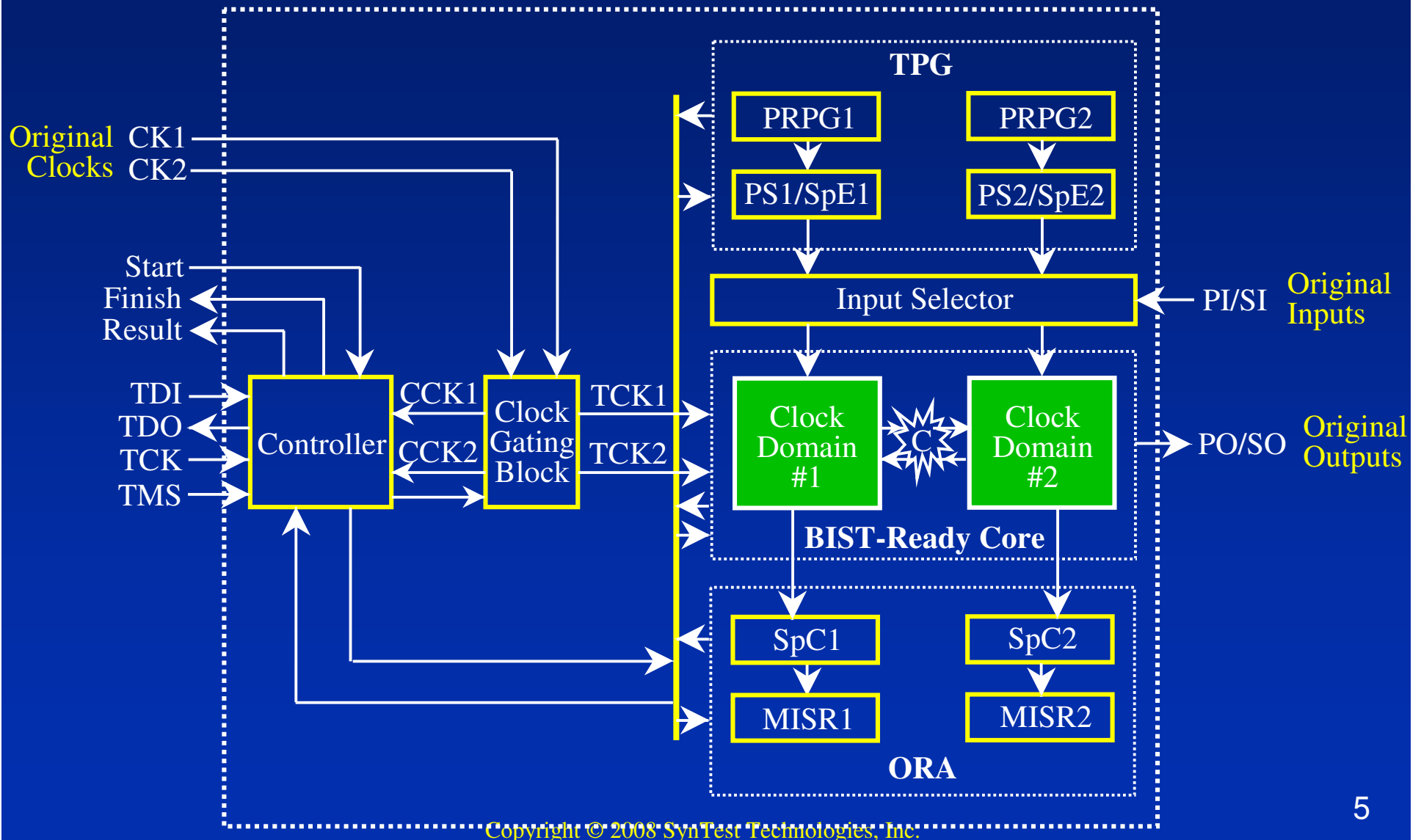
# Company Background

- SynTest was founded in January 1990.
- Develops and markets advanced **Design for Test (DFT) software** to improve the Product Quality and reduce Test Cost of IC designs.
- About **50 employees** in the U.S., Taiwan, Korea, Japan, and China.
- Approximately **60 customers** worldwide, including more than **15 DFT IP customers** since Oct. 2005.
- Has filed more than **38 patents** since 2001 of which **17 patents** are issued and **1 allowed**.

# SynTest Patent Portfolio

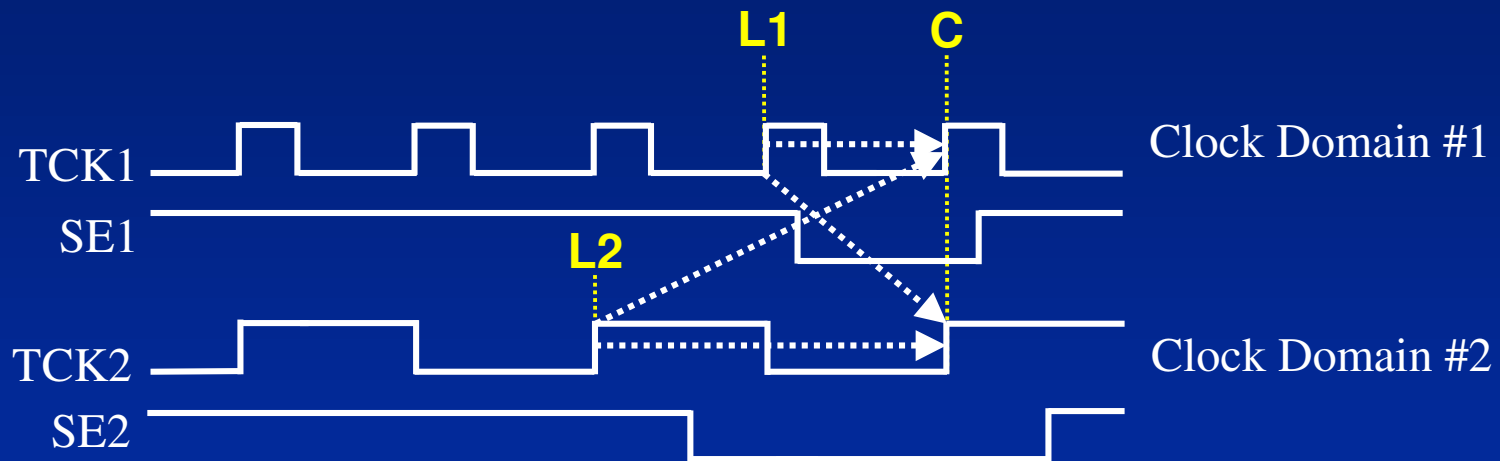
Patent Category	Patents Issued	Patents Allowed	Patents Pending	Patents Subtotal
At-Speed Staggered Double-Capture	3	0	1+	4+
At-Speed Staggered Skewed-Load	2	0	1+	3+
Test Compression	2	0	13+	15+
Automatic Test Pattern Generation	4	0	3+	7+
DFD	4	0	2+	6+
Memory Built-In Self-Test (BIST)	1	0	0	1+
Random-Access Scan Protection	0	1	0	1+
Analog BIST	1	0	0	1+
<b>Total Patents</b>	<b>17</b>	<b>1</b>	<b>20+</b>	<b>38+</b>

# Logic BIST Architecture



# Test Timing Control - 1

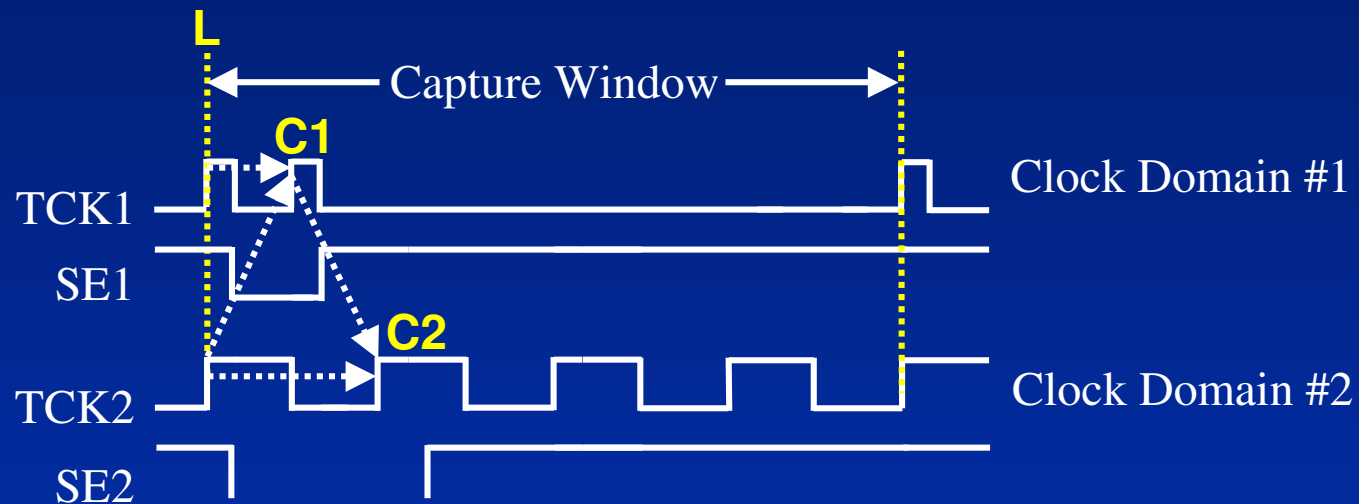
## Capture Aligned Skewed-Load (LogicVision Patent)



- Detect stuck-at & delay faults in each clock domain.
- Detect stuck-at & delay faults in all crossing-clock-domain logic blocks.
- **Require multiple at-speed SE signals.**
- Require strict crossing-clock-domain clock skew management.
- **No true at-speed testing when there are unrelated clock frequencies.**

# Test Timing Control - 2

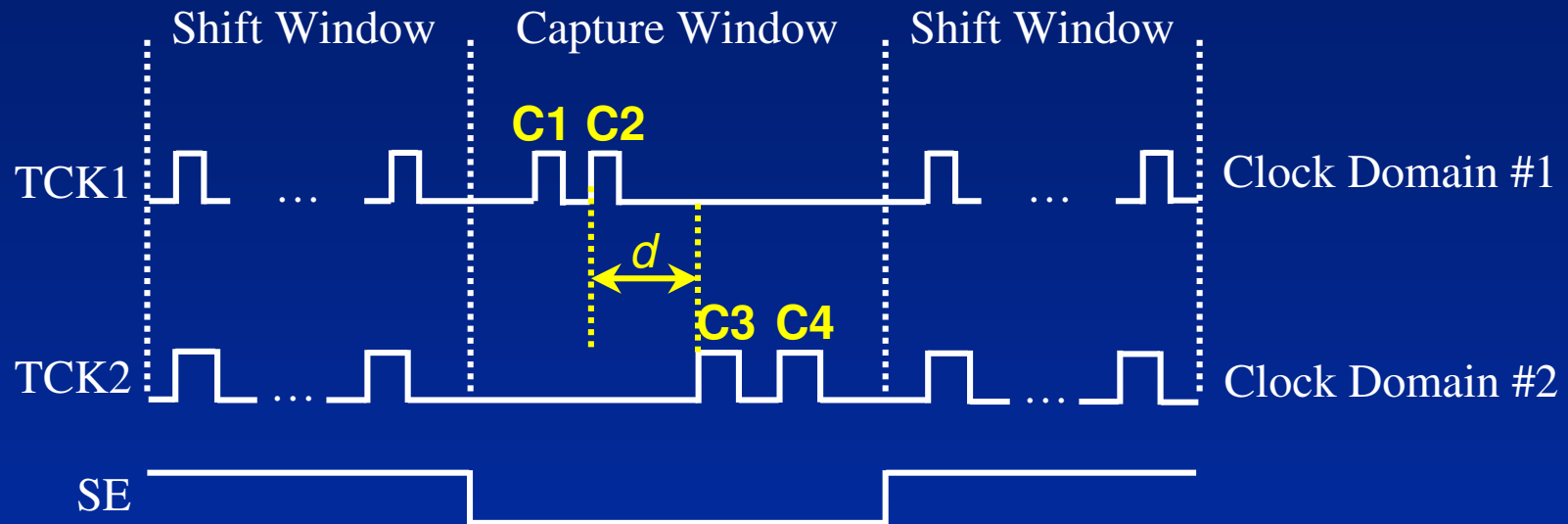
## Launch Aligned Skewed-Load (Mentor Patent)



- Detect stuck-at & delay faults in each clock domain.
- Detect stuck-at & delay faults in all crossing-clock-domain logic blocks.
- **Require multiple at-speed SE signals.**
- **No true at-speed testing when there are unrelated clock frequencies.**

# Test Timing Control - 3

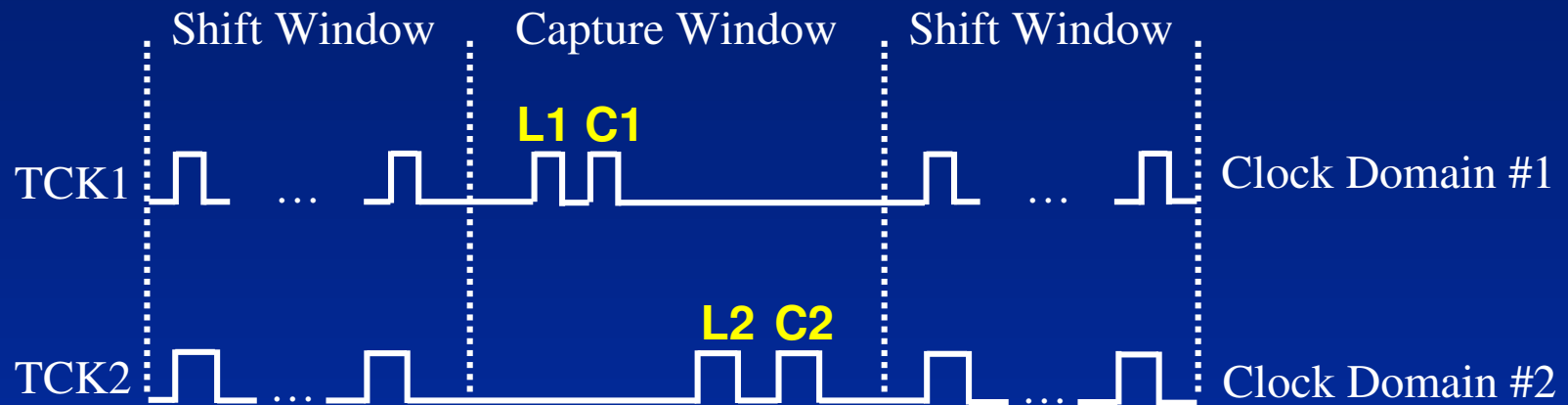
## Staggered Double-Capture (SynTest Patent)



- Detect stuck-at & delay faults (clock domain #1).
- Detect stuck-at & delay faults (clock domain #2).
- Detect stuck-at faults (clock domain #1 → clock domain #2)
- Detect delay faults (clock domain #1 → clock domain #2) for proper  $d$ .
- **Need only one single and slow SE signal.**
- **True at-speed testing when there are unrelated clock frequencies.**

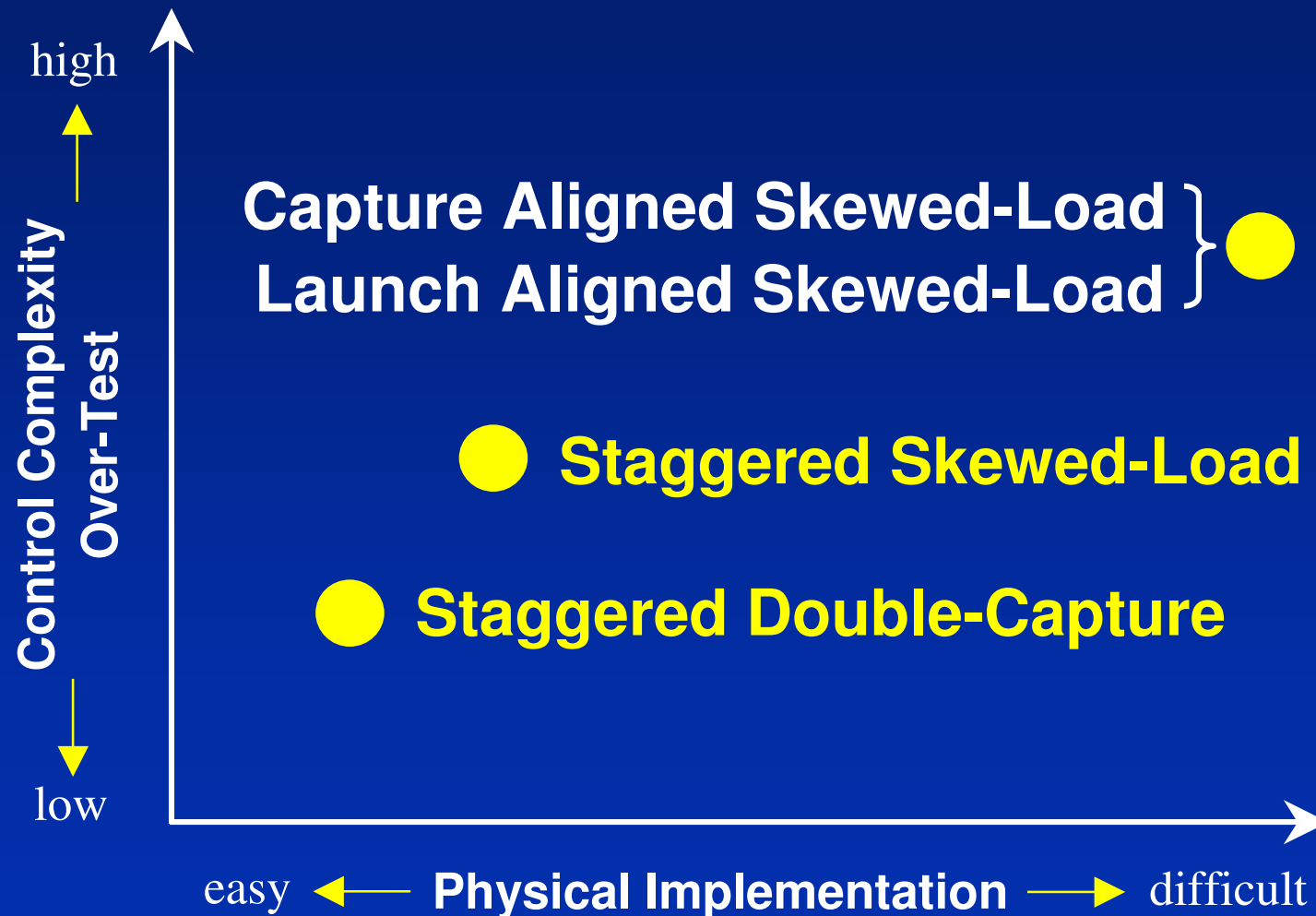
# Test Timing Control - 4

## Staggered Skewed-Load (SynTest Patent)

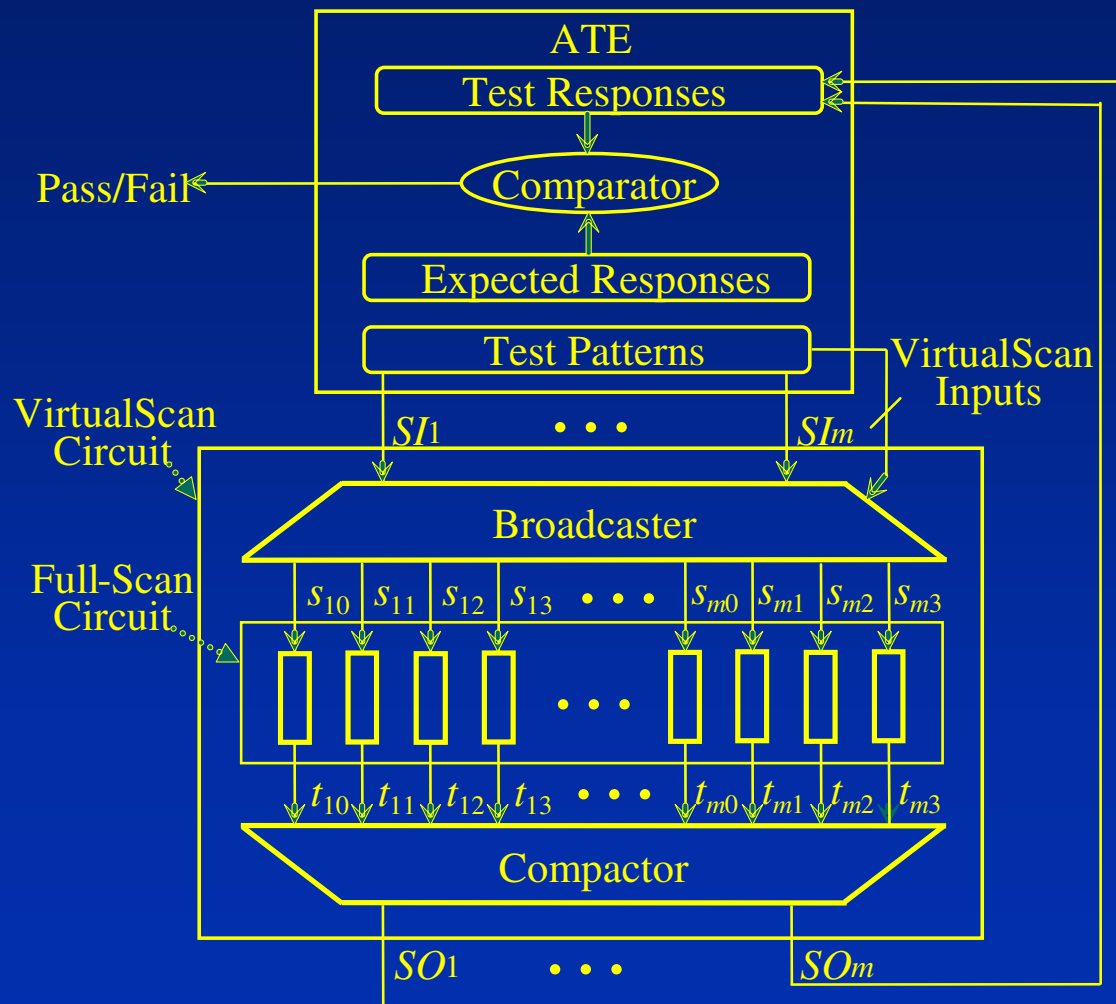


- Detect stuck-at & delay faults (clock domain #1).
- Detect stuck-at & delay faults (clock domain #2).
- Detect stuck-at faults (clock domain #1 → clock domain #2)
- Require multiple at-speed SE signals.
- True at-speed testing when there are unrelated clock frequencies.

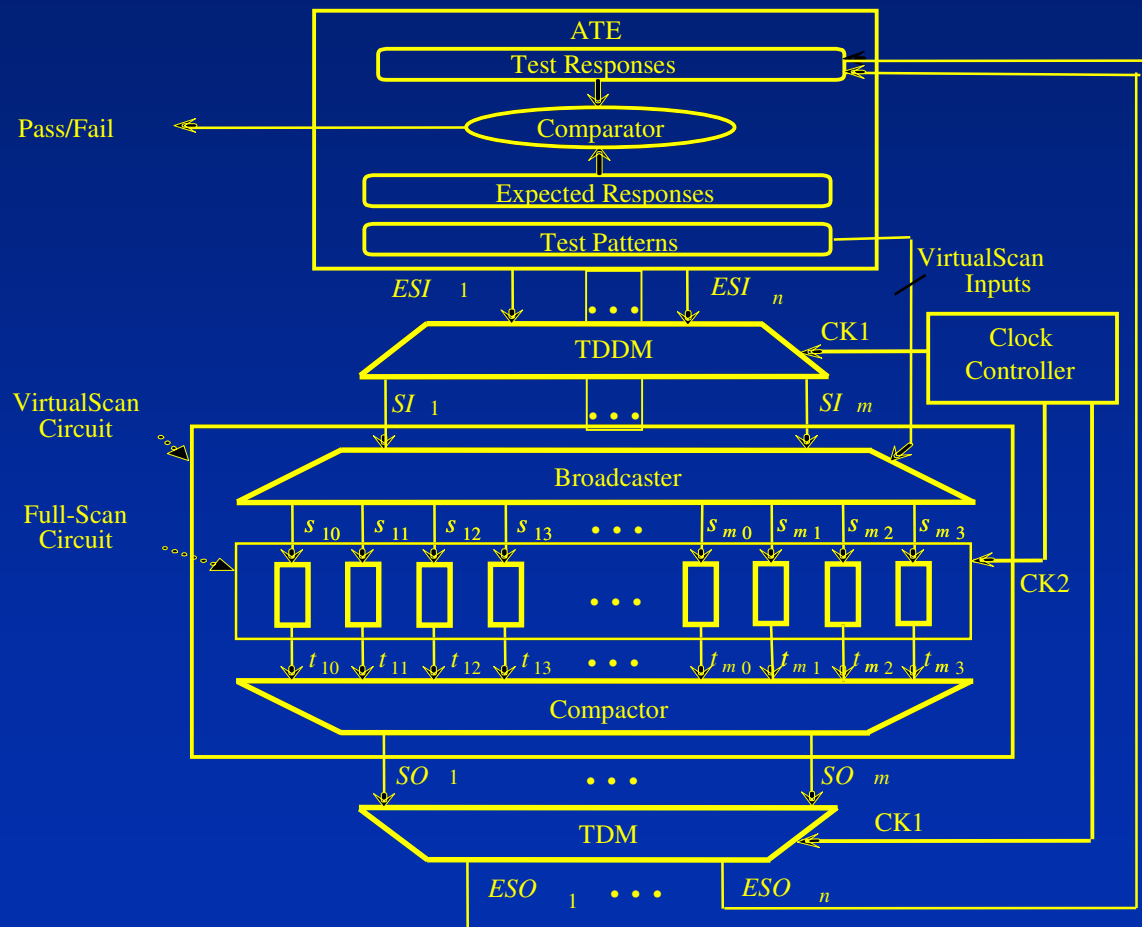
# Comparison



# VirtualScan Architecture (SynTest Patent)



# UltraScan Architecture (SynTest Patent)



# Comparison (Test Compression)

Test Compression	VirtualScan & UltraScan (SynTest)	DFT MAX (Synopsys)	TestKompress (Mentor)	OPMISR+ (Cadence)
Decompressor	TDDM/XOR network	MUX network	LFSR-based	XOR network
Compactor	XOR/TDM network	XOR network	XOR network	MISR+XOR network
Test Time Compression	100x-1000x	10x-50x	10x-50x	10x-50x
U.S. Patents	Pending (SynTest)	-	Rajski et al. (Mentor)	Koenemann et al. (IBM)

# Comparison (At-Speed Testing)

At-Speed Testing	TurboScan TurboBIST (SynTest)	TetraMAX (Synopsys)	FastScan (Mentor)	LV2005 (LogicVision)
Staggered double-capture	√			
Staggered skewed-load	√			
Capture aligned skewed-load				√
Launch aligned skewed-load			√	
U.S. Patents	Wang et al. (SynTest)	-	Rajski et al. (Mentor)	Nadeau-Dostie et al. (LV)

# Conclusions

- 17 patents issued
  - Staggered skewed-load for At-speed Scan and Logic BIST (U.S. Pat. No. 6,954,887)
  - RTL scan synthesis (U.S. Pat. No. 6,957,403)
  - Staggered double-capture for At-speed Logic BIST (U.S. Pat. No. 7,007,213)
  - X-mask network design (U.S. Pat. No. 7,032,148)
  - DFD and DFY for scan and BIST cores (U.S. Pat. No. 7,058,869)
  - Scan Automatic Test Pattern Generation [ATPG] (U.S. Pat. No. 7,124,342)
  - Diagnosing Failures in an IC Using DFD Techniques (U.S. Pat. No. 7,191,373)
  - ATPG and Fault Simulation in a Scan-Based IC (U.S. Pat. No. 7,210,082)
  - IEEE std. 1149.4 Compatible Analog BIST Methodology (U.S. Pat. No. 7,228,479)
  - Multi-level Test Compression (U.S. Pat. No. 7,231,570)
  - Staggered double-capture for At-speed Scan (U.S. Pat. No. 7,260,756)
  - Diagnosing failures in an IC using DFD techniques (U.S. Pat. No. 7,284,175)
  - System to Automate Scan Synthesis at RTL (U.S. Pat. No. 7,331,032)
  - Staggered skewed-load for At-speed Scan (European Pat. No. 1,360,513) – UK, Germany and France)
  - DFD for scan cores (European Pat. No. 1,364,436) – UK, Germany and France)
  - Multiple-Capture DFT system for Scan (European Pat. No. 1,370,880) – UK, Germany and France)
  - Optimize Test Cost and Disable Defects (European Pat. No. 1,377,981) – UK, Germany and France)
- 1 patent allowed
  - Broadcasting scan patterns in a Random Access Scan based Integrated Circuit
- Patents pending – Test Compression patents

# Conclusions (Cont'd)

- Transition from a Tool vendor to a DFT IP provider
  - to partner with end users
  - to partner with EDA, library, and IP vendors
  - to partner with ATE and design service houses
- **Business Model**
  - Licenses DFT/DFD patents & architectures for annual fee
  - Per design fee for using test compression or logic BIST IP
- **Training and consulting services** when requested
- **The DFT textbook** (808 pages) published by Elsevier in July 2006 titled *VLSI Test Principles and Architectures*
- **The DFX textbook** (896 pages) published by Elsevier in November 2007 titled *System-on-Chip Test Architectures*
- **The EDA textbook** to be published by Elsevier in Dec. 2008 titled *Electronic Design Automation: Synthesis, Verification, and Test*