SynTest Reduces the Cost of Semiconductor Testing

VirtualScan’s compaction technology extends life of existing ATE for large SOC designs

SUNNYVALE, California, Sept. 3, 2002 – Design-for-Test (DFT) leader SynTest Technologies today announced a software product called VirtualScan™.

VirtualScan offers a significant reduction in the cost of semiconductor testing by reducing test data volume, test run time and Automatic Test Equipment (ATE) reloads. An evaluation on a 2-million gate circuit showed a 15x reduction in test time.

VirtualScan employs a proprietary, patent-pending compaction technology that allows existing ATE resources to apply ATPG patterns through each external scan chain to a user-selectable, larger number of shorter internal scan chains. Using a large number of short scan chains reduces test application time and ATE memory storage requirement, without compromising product quality and extends the utilization of existing ATE for larger chip sizes.

“We have been at the forefront of the fight to not let pattern size get out of hand with our proprietary static and dynamic compaction technologies. Hence, in spite of the ever increasing complexity and size of SOC designs, our customers have been kept relatively immune to the exploding test costs," remarked Dr. L.-T. Wang, President and CEO of SynTest Technologies.

About Scan and Semiconductor Test
SOC semiconductor testing cost has been increasing steadily over the past few years and is now a major part of the overall manufacturing cost of chips. With the average SOC design size expected to grow to greater than 5 million gates in the near future, a new approach such as SynTest’s VirtualScan is needed to reduce test application time and test data volume.
What’s VirtualScan

With SynTest’s VirtualScan, an extremely large number of short scan chains within the SOC can be virtually accessed from outside the chip with a limited number of pins assigned as scan pins. Inside the chip, SynTest’s new patent-pending circuitry is used to broadcast each external scan-input chain to a user-selectable number of internal scan chains and at the other end, compact them into the original number of external scan chains.

VirtualScan contains an automatic synthesizer to incorporate the broadcaster and compactor into the scan circuitry and uses broadcast ATPG technology to generate test patterns. It also contains tools for scan insertion and scan synthesis.

Integration into DFT/Test environments

VirtualScan does not require users to change their scan methodology. It’s fully compatible with SynTest’s existing DFT tools such as TurboCheck™ for DFT rule checking, TurboBIST-Memory™ for BISTing embedded memories, TurboBSD™ for boundary scan synthesis, TurboDFT™ for automatic integration of DFT blocks, TurboFault™ for concurrent fault simulation, as well as TurboDebug-SOC/Scan and TurboDiagnosis-Scan for debug, diagnosis and failure analysis of scan chains.

VirtualScan also works with netlists that have scan inserted using other popular scan-insertion tools.

Pricing and Availability

VirtualScan is currently available for beta-testing to select customers. It is expected to ship Q1/2003. Pricing beginning at US$250,000. An upgrade to VirtualScan is available to licensees of SynTest’s TurboScan™, a scan synthesis and ATPG product.

About SynTest:

SynTest Technologies, Inc. develops and markets advanced DFT and Design-for-Debug/Diagnosis (DFD) tools, throughout the world to semiconductor companies, ASIC designers and test groups. Headquartered in Sunnyvale, California, the company has offices in Taiwan, Korea and Japan. The Company’s products improve an electronic design’s testability and fault coverage and result in
reduced defect levels, reduced costly tester time, and reduced slippage in time-to-market. These products include tools for Built-in Self-Test (BIST) for logic and memory, boundary-scan synthesis, DFT testability analysis, scan synthesis, ATPG, concurrent fault simulation, silicon debug and diagnosis. More information is available at [www.syntest.com](http://www.syntest.com).

SynTest Technologies Inc. is headquartered at 505 South Pastoria Ave., Suite 101, Sunnyvale, California 94086, Phone: 408-720-9956, E-Mail: [info@syntest.com](mailto:info@syntest.com)

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**Acronyms:**
ATE: Automatic Test Equipment
ATPG: Automatic Test Program Generation
BIST: Built-In Self Test
BSD: Boundary Scan Design
DFD: Design for Debug/Diagnosis
DFT: Design For Test

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