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Test Data Compaction Tool from SynTest

VirtualScan™

An Application Story

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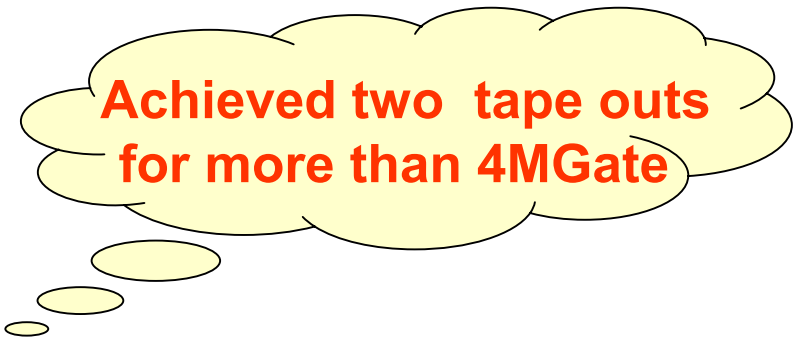
Agenda

- Current Problems
- What is VirtualScan?
- Trial Results for Real Designs
- Actual Application Results of Real Designs



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Current Problems

Test Cost Increase caused by LSI circuit size expansion

- **Test Cycle**
  - Test time increasing along with LSI circuit size
- **Test Pattern**
  - Pattern load overhead caused by larger test than pattern memory of ATE
- **Test Coverage – Co-mingling Ratio** (ratio of defective devices with good devices)
  - Omitting test patterns just for test cost reduction, results in sacrificing the co-mingling ratio
- **Moreover**
  - Transition delay patterns for delay fault detection in addition to patterns for stuck-at faults

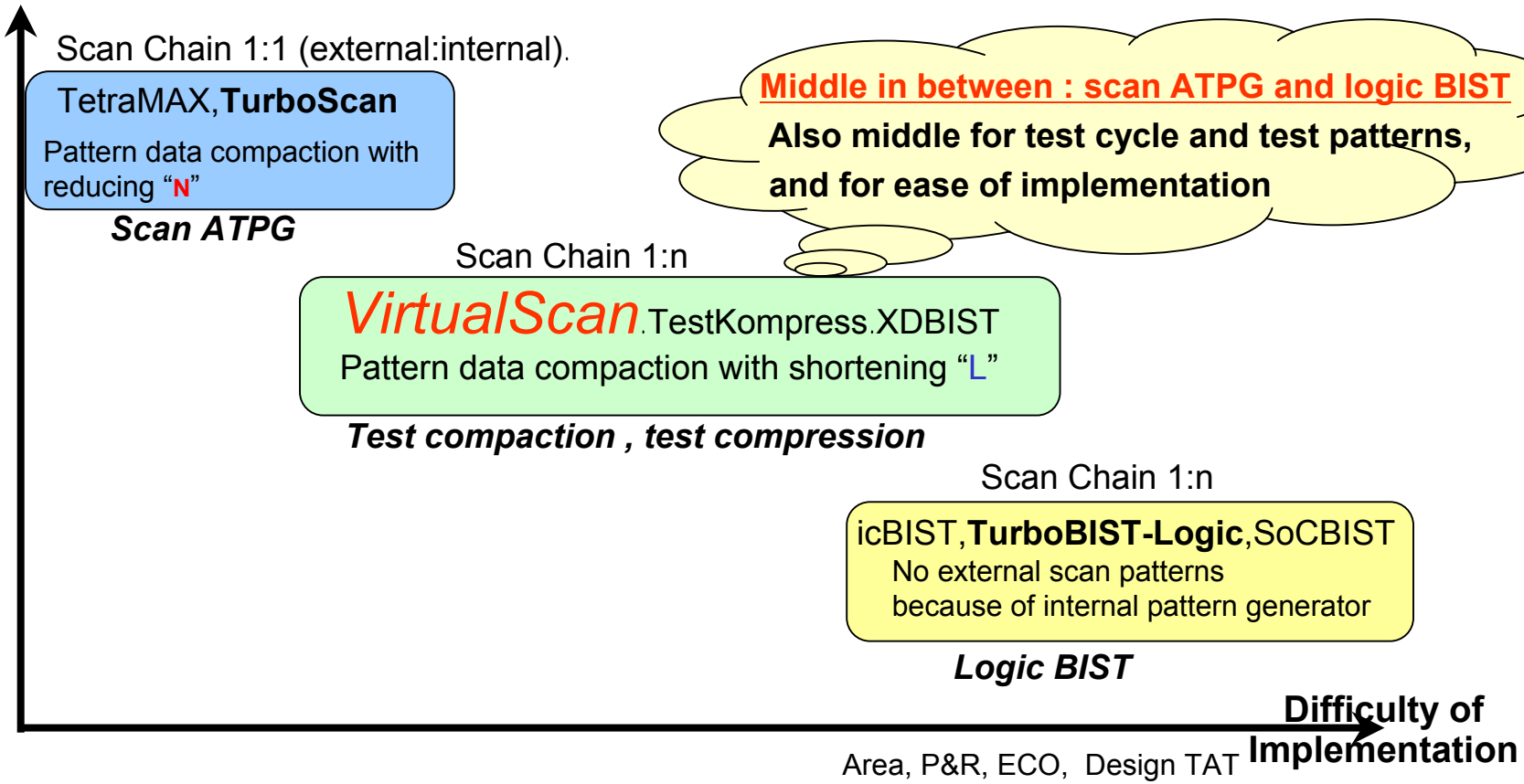
No solution, but to keep unending purchase to fit for LSI increase

Position of DFT Tools

- Comparison of methodology

Test cost { *Test Cycle Volume* N x L ; *Test Pattern Volume* N x L x W

N : number of patterns
L : scan chain length
W : number of scan chains



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What is most important in test compaction?

Why LBIST can't be so popular ?

- Difficult to implement
- Definitely LBIST is superior just for compression ratio

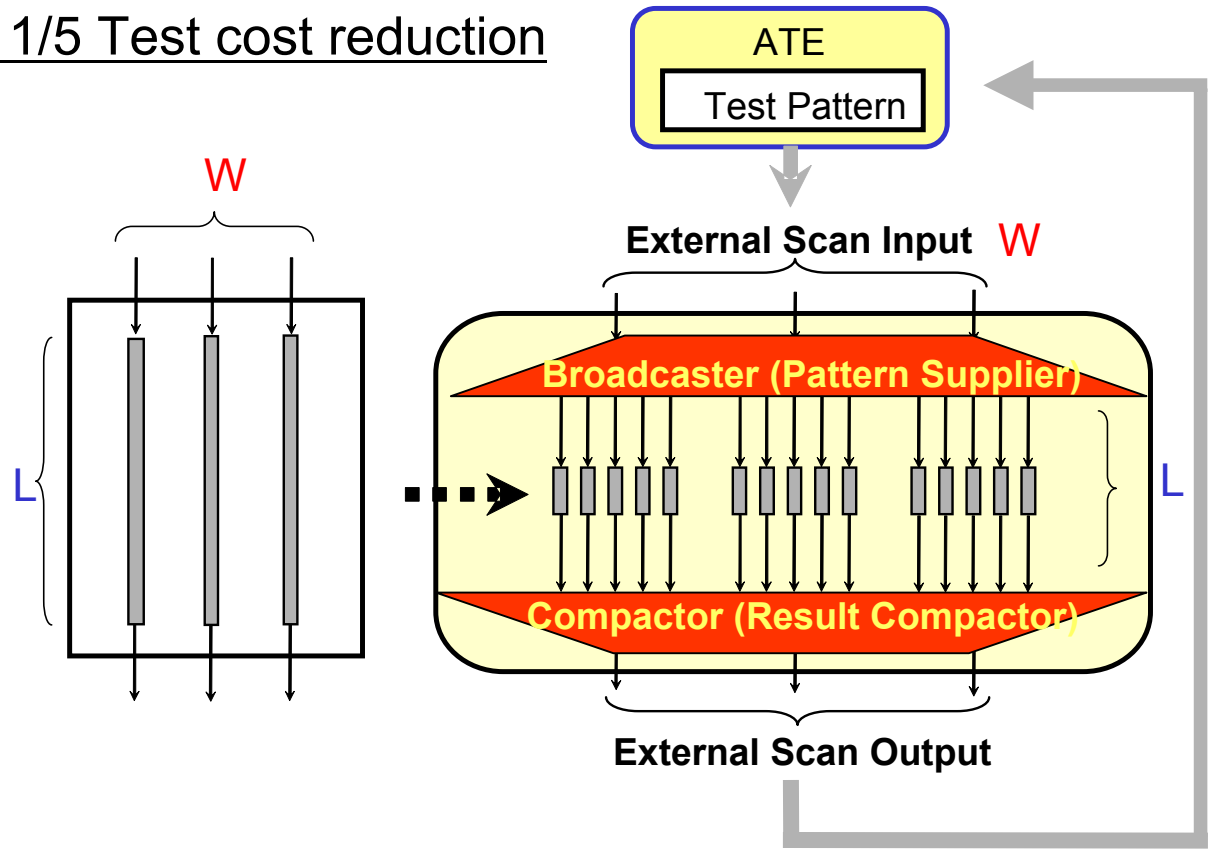
What is necessary for test compaction

- *Ease of Implementation*
- Above that, to get desired compaction ratio

What is VirtualScan™ ?

❒ Feature: Scan chain split (L reduction) and ATPG

(Ex) 1/5 Test cost reduction



Test cycle

N x L

N x 1/5 L

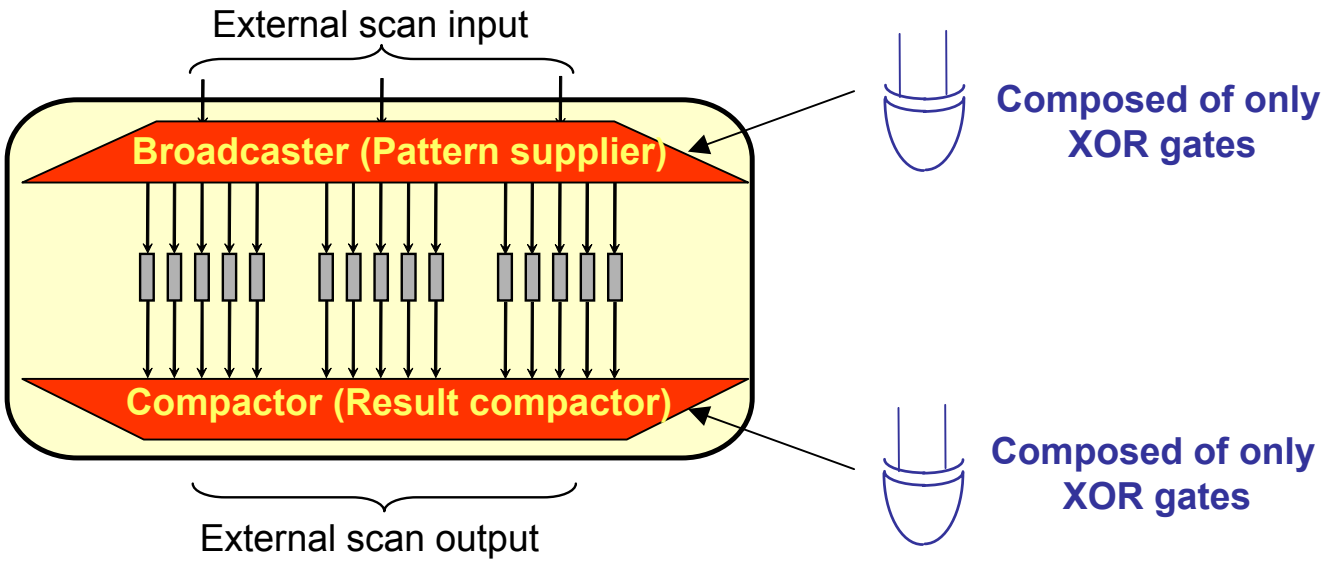
Pattern Volume

N x L x W

N x 1/5 L x W

Merits of VirtualScan™

- Additional logic is only gate circuit (XOR)
  - No need to modify clock, the most important factor in sequential circuits
  - No need to think about clock, fmax/hold of added circuit, and inter clock



- No need to modify functional logic. Only need to modify scan chains
  - Moreover, additional logic is only XOR between PI~REG and REG~OUT
- No additional pin
  - Only 1 additional pin just for Top-up ATPG (Mode change for normal or VS).

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Trial Results for Real Design A

❒ Design Overview

Circuit Size - Logic part	1.2M Gates
Number of clocks	31
Number of scan chains	28
Number of Scan FFs	102,647
Max. scan chain length	3,666

Hierarchical netlist

7 clock groups

14 times compaction with 20 split

7 times compaction with 10 split

❒ Result

		20 Split VirtualScan	10 Split VirtualScan	TurboScan
Test Quality	Test Coverage	92.03%	92.14%	92.14%
Test Cost Pattern volume	Number of patterns	3,128	3,065	2,207
	Pattern increasing ratio	1.4	1.4	1
	Pattern volume (in millions)	16.12	31.50	225.42
	Compaction ratio (times x)	0.07 (14X)	0.14 (7X)	1
Test cost - Test cycle	Number of test cycles	575,552	1,124,855	8,090,862
	Compaction ratio (times x)	0.07 (14X)	0.14 (7X)	1
Design impact	TAT - Circuit generation (h)	3	3	0
	TAT - Pattern generation (h)	28	12	15
	Increase in number of gates	4,879	2,354	0
	Area OH	0.4%	0.2%	0

On SUN Blade2000/2900, 900MHz

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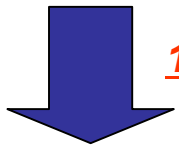
Trial Results for Real Design B

❒ Design Overview

Circuit Size - Logic part	4.2 M Gate	Flat netlist
Number of clocks	36	9 clock groups
Number of scan chains	30	
Number of Scan FFs	203, 578	
Max. scan chain length	7,005	



14 times compaction with 2 split

❒ Results

		VirtualScan	Existing ATPG
Test Quality	Test Coverage	92.61%	92.68%
Test Cost - Pattern volume	Number of patterns	2,546	19,094
	Pattern volume (in millions)	312.85	4379.71
	Compaction ratio (times x)	0.07	1
Test cost - Test cycle	Number of test cycles	9,529,678	133,829,846
	Compaction ratio (times x)	0.07 (14X)	1
Design impact	TAT - Circuit generation (h)	3	0
	TAT - Pattern generation (h)	182	89
	Increase in number of gates	344	0
	Area OH	0.01%	0

On SUN Blade2000/2900, 900MHz

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Trial Results for Real Design C

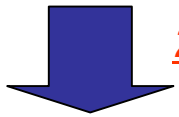
❒ Design Overview

Circuit Size - Logic part	4.5M Gate
Number of clocks	52
Number of scan chains	32
Number of Scan FFs	250,364
Max. scan chain length	7,824

Hierarchical netlist

12 clock groups

❒ Result



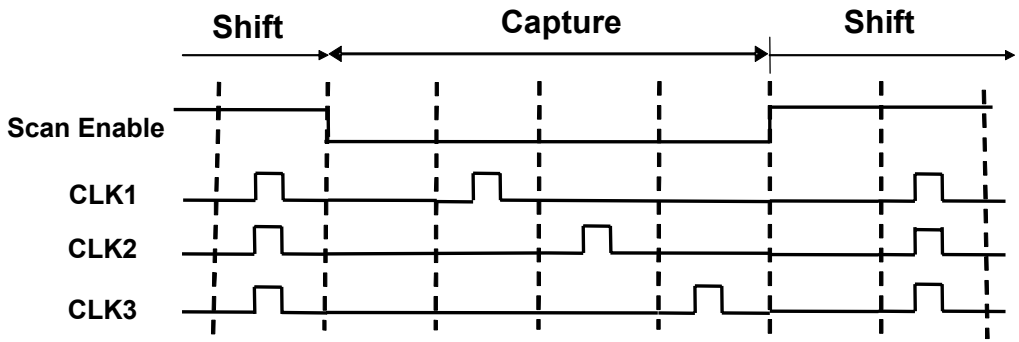
20 times compaction with 4 split

		VirtualScan	Existing ATPG
Test Quality	Test Coverage	97.15%	97.49%
Test Cost - Pattern volume	Number of patterns	4,472	21,041
	Pattern volume (in millions)	293.08	5343.40
	Compaction ratio (times X)	0.05 (20X)	1
Test cost- Test cycle	Number of test cycles	8,809,840	164,708,948
	Compaction ratio (times X)	0.05 (20X)	1
Design impact	TAT - Circuit generation (h)	1	0
	TAT - Pattern generation (h)	273	101
	Increase in number of gates	899	0
	Area OH	0.02%	0

On SUN Blade2000, 990MHz

MultiCapture

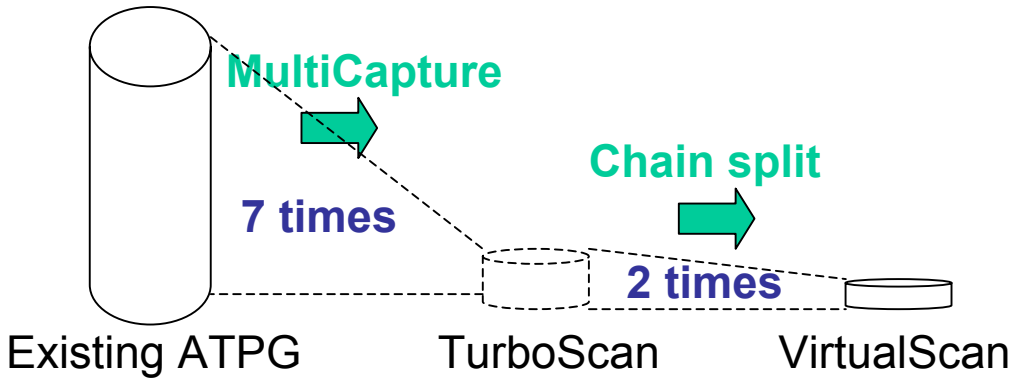
- Default feature through SynTest tools, which show a differentiation
  - All clocks are to be activated in order in one capture
  - It enables drastic pattern number compaction than other tools



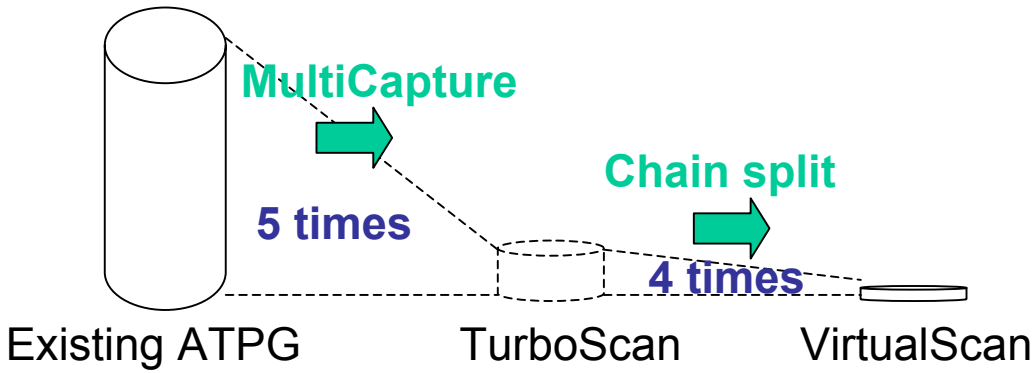
- Issue
  - Need more CPU and memory

Compaction Ratio

❒ Design B ***14 times compaction with 2 split***

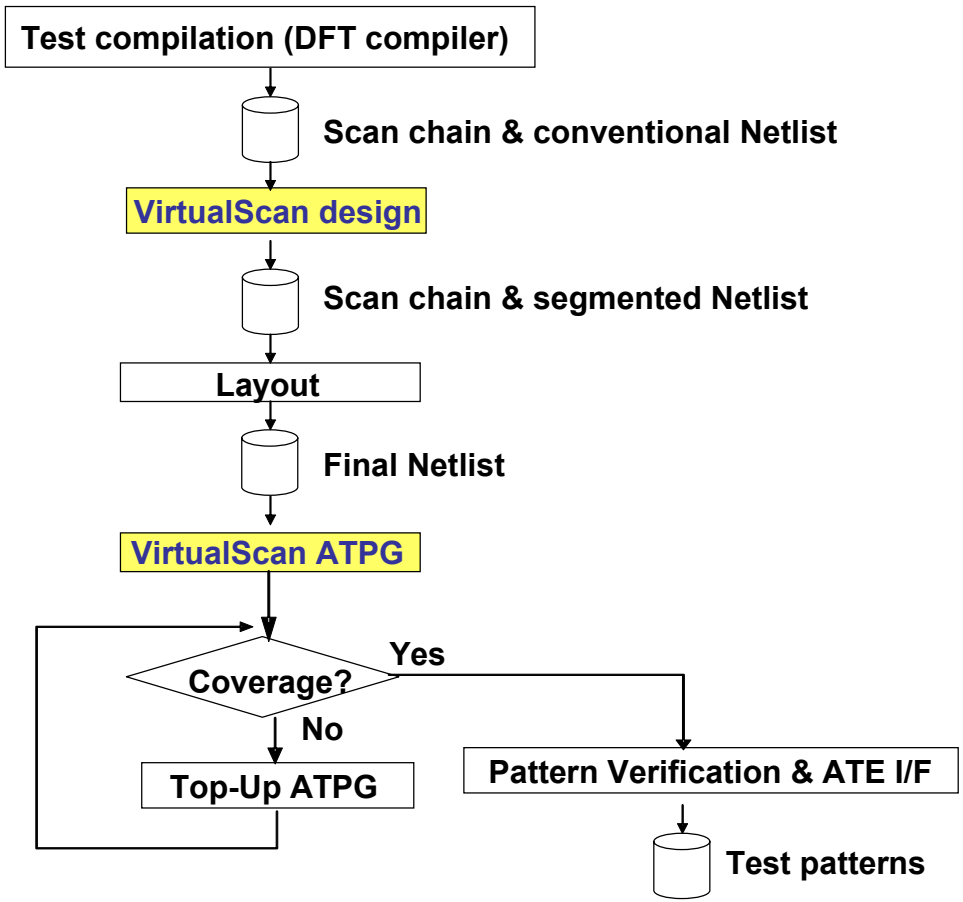


❒ Design C ***20 times compaction with 4 split***



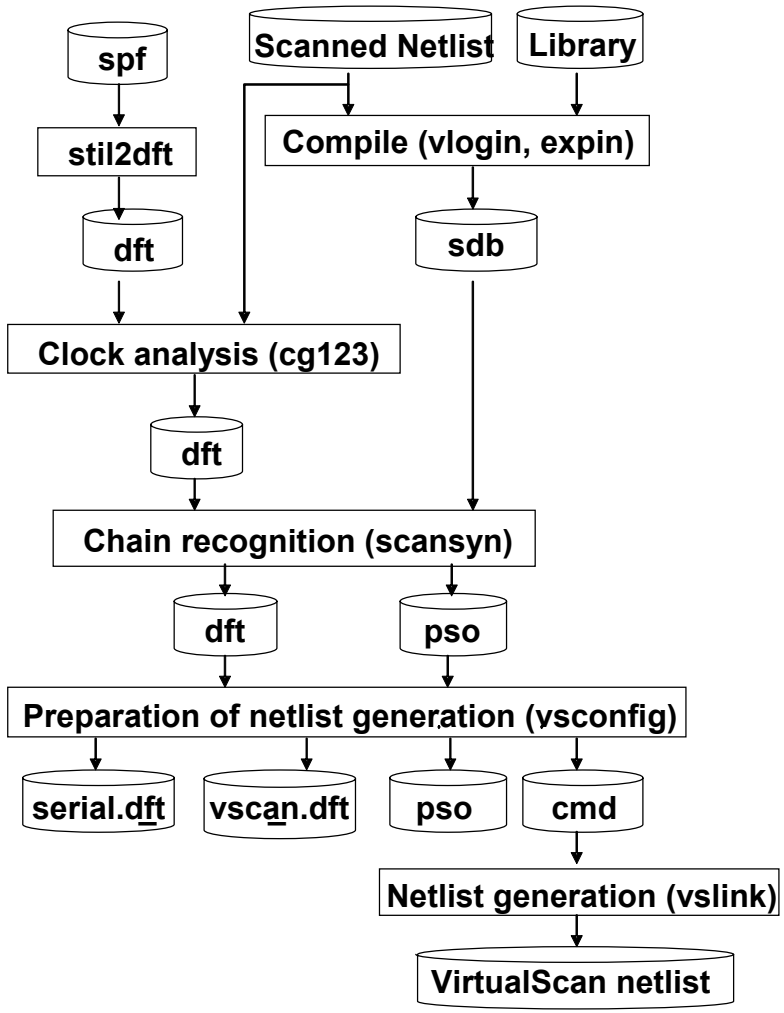
Design Flow with VirtualScan

- Netlist generation for VirtualScan is between test compilation & layout



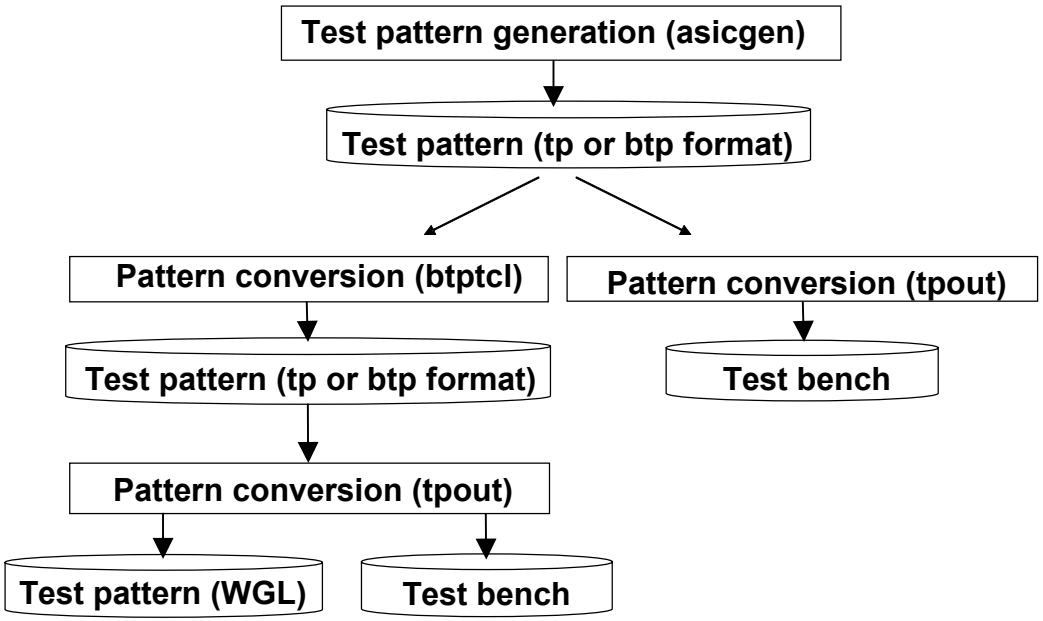
VirtualScan Process Flow – (1/2)

- VirtualScan Netlist generation



VirtualScan Process Flow – (2/2)

- ATPG - ATE Interface



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Summary

- Easy to implement
  - Circuit added is just combinational, so no clock care needed
- Small area overhead
  - Less than 1%, depending only on split number, and easy to estimate
- Short implementation TAT
  - Only 1-3 hours even for 4M gate design
- Long TAT for ATPG, (but short TAT for top-up ATPG)
  - 7-11 days for design with 4M gates & 10 clock group
- Slightly lower fault coverage (vs. scan ATPG)
  - However, Top-Up ATPG enables to get same coverage as scan ATPG
- Predictable compaction ratio
  - Scan ATPG-like, and almost proportional to split ratio

Applicable to all LSI circuits from small one to big one

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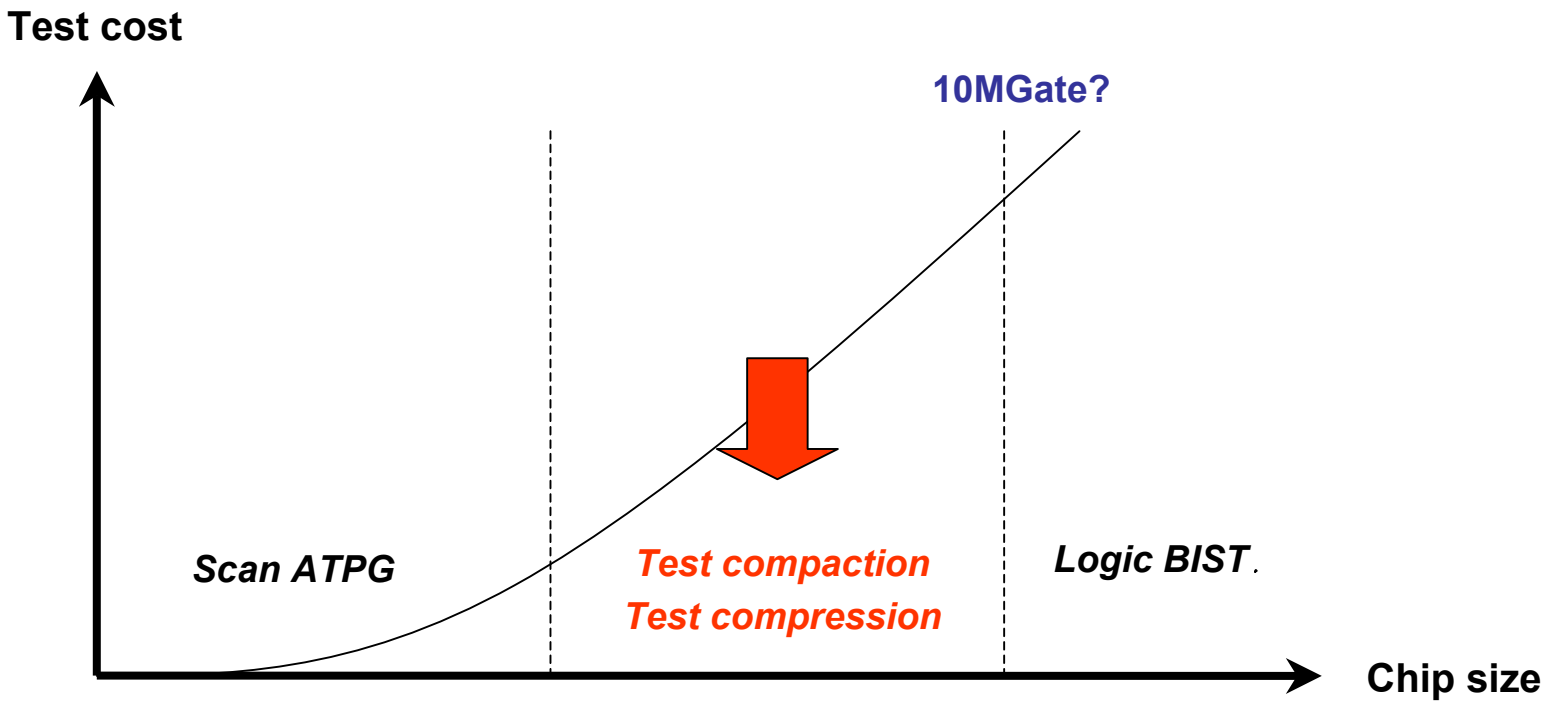
Action Items

- To run more chain splits (in progress)
  - To split 10 to 20 to confirm higher compaction ratio
- To run with distributed ATPG environment (in progress)
  - Shorten large ATPG TAT
- To apply transition delay ATPG to real design (in progress)
  - To reject delay faults in real devices
- To run with transition delay fault with PLL circuit (Q1)
  - To Enable At-speed test exceeding ATE clock frequency
- To confirm Integration with MAGMA Blast Fusion (Q1)
  - To realize physical synthesis of RTL-to-GDS
- To integrate with logic BIST (Q2)
  - TurboBIST-Logic and top-up ATPG by VirtualScan

Many bugs were found initially because it was new, but has matured recently.

DFT Tools Segmentation

- Test compaction is enough for current LSI size



- Is LBIST only for board test?

NECマイクロシステム

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