



SYNTEST

The Testability Company

BENEFITS

- Automatically performs IEEE 1149.1 compliant boundary scan logic synthesis
- Automatically generates boundary scan description language (BSDL) files
- Automatically generates boundary scan test patterns, including verification and parametric test benches
- Supports RTL or gate level netlist generation in Verilog and VHDL formats
- Form-based boundary scan description entry for fast, error free operation
- Reduces boundary scan design time to minutes per design

PRODUCT DESCRIPTION

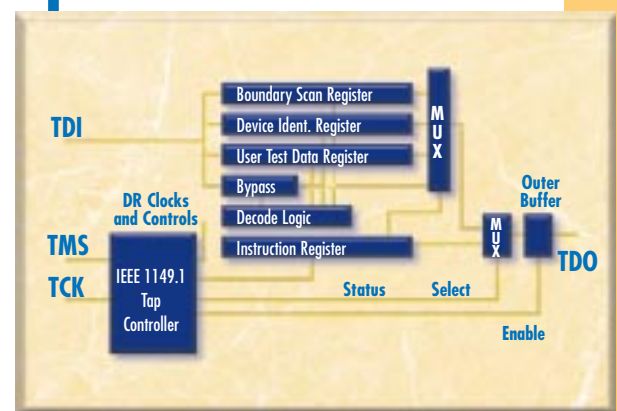
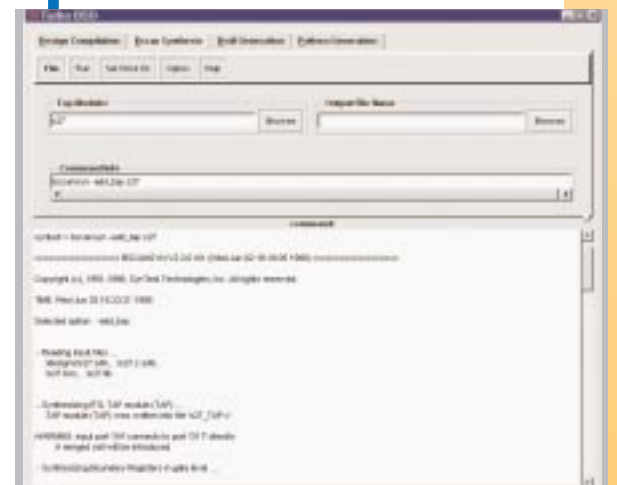
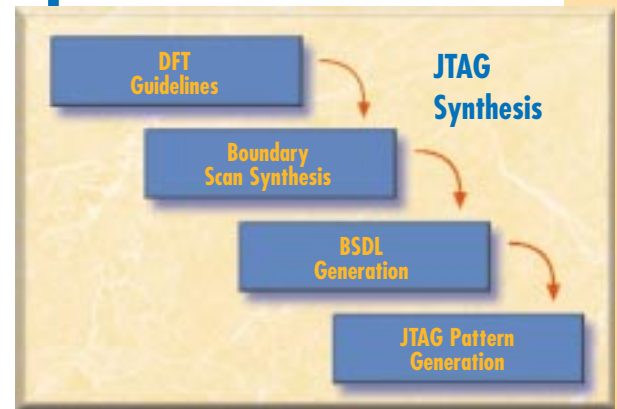
TurboBSD is a high performance boundary scan design suite that makes boundary scan design a fast and straightforward process. It synthesizes boundary scan cells, the TAP controller and instruction registers. The tool can output synthesizable Verilog and VHDL RTL codes that can be customized for your application and later synthesized using your own technology libraries. In addition to the standard IEEE 1149.1 public instructions, TurboBSD also supports custom ID code and private instructions. After synthesis, it extracts the boundary scan chain information from the circuit and automatically creates the correct BSDL file. TurboBSD automatically generates implementation and fault model independent functional test sets to verify the integrity of the boundary scan logic. TurboBSD also generates parametric tests (e.g., V_{OH} , V_{OL} , V_{IH} , and V_{IL}), and generates test patterns to control BIST operations using test information in the SVF format.

PLATFORMS

TurboBSD runs on SUN Solaris, HP-UX and Linux platforms and it supports both Verilog and VHDL.

OTHER INFORMATION

TurboBSD reads Verilog and VHDL formats and outputs either RTL or cell level netlists. It also provides Verilog and VHDL test benches. The three main functions of TurboBSD are implemented so as to allow designers to use other EDA tools for boundary scan synthesis while still providing BSDL file generation and test pattern generation capabilities.



SynTest Service and Support

APPLICATIONS ENGINEERING

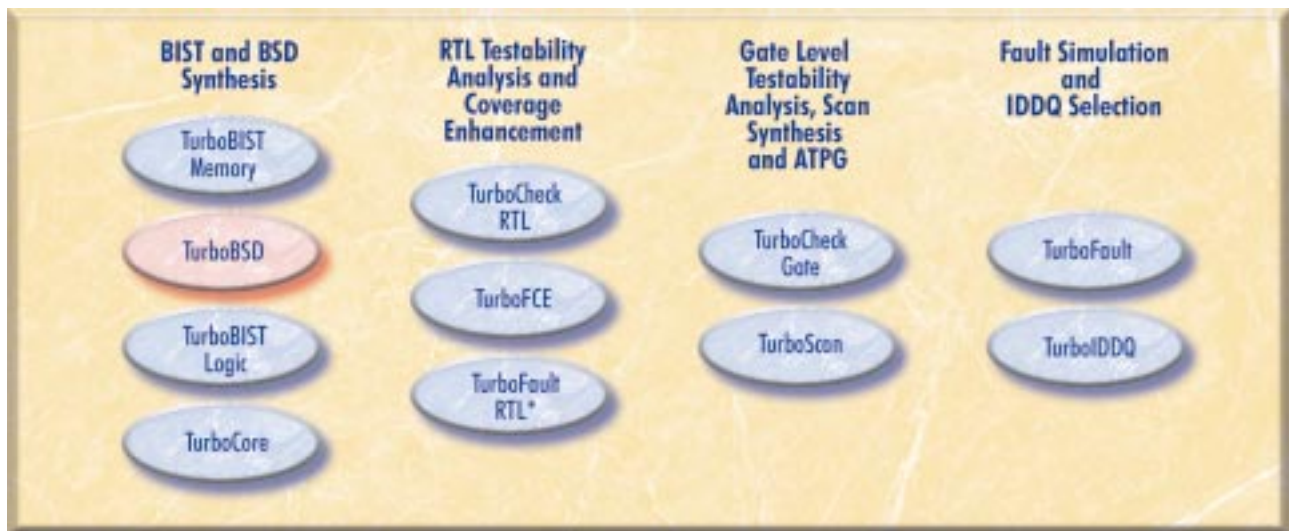
Part of the mission of the Applications Engineering Group is to help our customers to become their own experts in using our tools. Test synthesis is not a 'push button' process. SynTest tools will make the process much easier. Customers who do not have too much experience in this area can usually use our help to 'kick-start' their projects. The Application Engineering group can provide tools and methodology training at the beginning of the design cycle. During tape-out, we are also available to help with any final critical problems related to test synthesis. Our goal is to have our customers feel that they are not alone after they purchase our tools. We are always there to help.

CONSULTING ENGINEERING

In addition to direct product sales, part of SynTest's company mission is to emphasize excellent support for our customers. Our Consulting Engineering Group provides test synthesis and ATPG expertise to our customers who may not have enough resources to accomplish these tasks. We provide a wide range of services from design flow methodology integration to a complete turn-key solution for our customers. We have expertise in testability analysis, test synthesis, ATPG, and fault simulation. Our past service projects include Pentium class CPUs, advanced 3D Graphics chips, network communication devices, etc. Please contact SynTest for more information on our Consulting Services.

THE SYNTTEST PRODUCT FAMILY

The SynTest product family is an ever-growing suite of high quality advanced tools to help you keep pace with the ever-changing requirements for test design, design for test, ATPG, fault simulation and other state-of-the-art testability solutions. If we don't have it today, we'll partner with you to develop it specifically for your needs.



*Available Mid-1999



SYNTTEST

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Offices and Distributors Worldwide -- Please call, e-mail or visit our web site for the one closest to you. <http://www.syntest.com>

Corporate Headquarters:
SynTest Technologies, Inc.
505 S. Pastoria Ave., Suite 101
Sunnyvale, CA 94086

Telephone: 408.720.9956
Facsimile: 408.720.9960
E-Mail: info@syntest.com