VirtualScan™

TOOL SUITE FOR VIRTUAL SCAN SYNTHESIS AND ATPG (AUTOMATIC TEST PATTERN GENERATION)

SYNTEST

The Testability Company

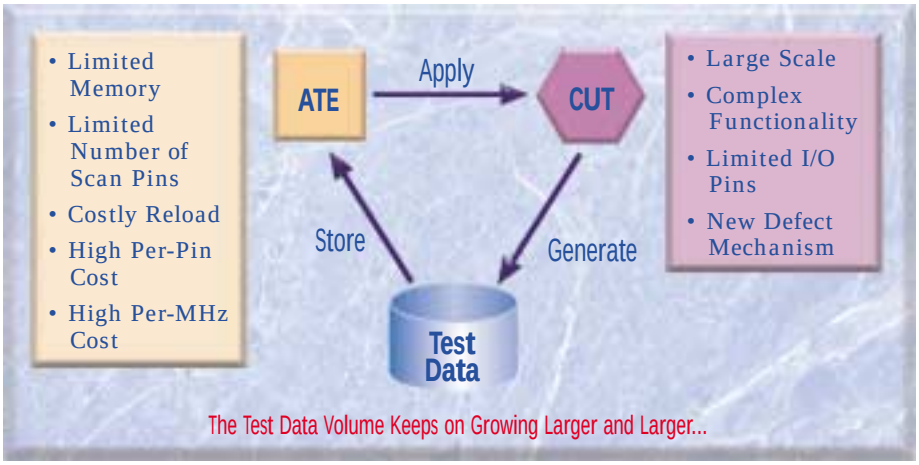
Today, integrated chips with multi-million gates, containing logic, memory and analog functions, are becoming commonplace. At the same time, meeting tight time-to-market schedules, controlling costs and maintaining high quality standards are critical to the success of any such new development.

Design-for-Test (DFT) tools and methodologies enable automation of many aspects of the structural testing process, ensuring that the chip comes through tape-out and manufacturing on time and according to specifications with acceptable level of quality. Among the various DFT methodologies available today for structural testing, scan insertion with Automatic Test Pattern Generation (ATPG) is the most preferred DFT methodology.

However, semiconductor-testing cost has been increasing steadily over the past few years to make it today a major part of the overall manufacturing cost of chips. The rapidly increasing size and complexity of new chips calls for a radical approach to enable companies developing million-gate System-on-Chips (SOCs) to speed their products through the test process more rapidly without having to upgrade to more expensive, next generation Automatic Test Equipment (ATE) or expand existing ATE scan pattern memory.

The diagram below shows the relationship between a Chip-Under-Test (CUT), the test data generated and the ATE. On one hand, the ATE limitations include limited number of scan pins, limited amount of scan pattern memory, high per-pin cost as well as high per-MHz cost. On the other hand, new SOC designs are larger in size, have complex functionality, limited number of I/O pins and due to shrinking geometries need to test more different types of defects, calling for bigger pattern sizes, longer scan chains and ever-increasing test data volumes to attain high fault coverage. However, bigger pattern sizes need more scan pattern memory and longer scan chains need longer test time, both resulting in higher test costs.

VirtualScan™ is SynTest's solution to combat this increase in test data volume and test cycle volume. With VirtualScan™ an extremely large number of short scan chains within the SOC can be virtually accessed from outside the chip with a limited number of pins assigned as scan pins. Inside the chip, SynTest's new patent-pending circuitry is used to broadcast each external scan-input chain to a user-selectable number of internal scan chains and at the other end, compact them into the original number of external scan chains. An evaluation on a 2-million gate design using VirtualScan™ showed a 22x reduction in test time. Further, the static and dynamic compaction capabilities of SynTest's powerful ATPG tool help reduce pattern sizes, leading to overall reduction in test costs.



BENEFITS OF VIRTUALSCAN™

- Reduces cost of semiconductor testing – 5x to 50x
- Extends life of existing ATE for large SOC designs
- Smaller test data volume and shorter test time
- Short test development time with no iterations
- High fault coverage
- Predictable and very low hardware overhead
- Smooth migration into existing scan ATPG flow
- Diagnosis support

FEATURES OF VIRTUALSCAN™

- Patent-pending virtual scan technology for broadcasting external scan chains to a user-selectable number of shorter internal scan chains and compacting them back into original number of external scan chains
- Automatically inserts broadcaster and compactor circuitry
- Outputs complete virtual scan netlist
- Includes tools for scan insertion and synthesis
- Uses an enhanced virtual scan ATPG
- Static and dynamic compaction of ATPG patterns
- Advanced multiple clock domain handling using proprietary multiple-capture-per-cycle scheme
- Can be used with scan chains inserted using third party tools
- Fully compatible with SynTest's existing DFT tools as well as TurboDebug-SOC/Scan and TurboDiagnosis-Scan for scan debug, diagnosis and failure analysis

TEST COST REDUCTION

In a scan test environment, the test cost depends on the test data volume and the test cycle volume.

The test data volume determines the pattern memory required on an ATE. To process increasing test data volumes, the options are either to increase pattern memory size which is expensive, or run reloads on the ATE, which means more time of ATE usage, again resulting in increased costs.

The figure alongside illustrates the relationships that affect these test costs, where
N = Number of scan test patterns
L = Scan chain length
W = Width of stored patterns

Hence, to reduce the test costs we need to reduce both N and L.

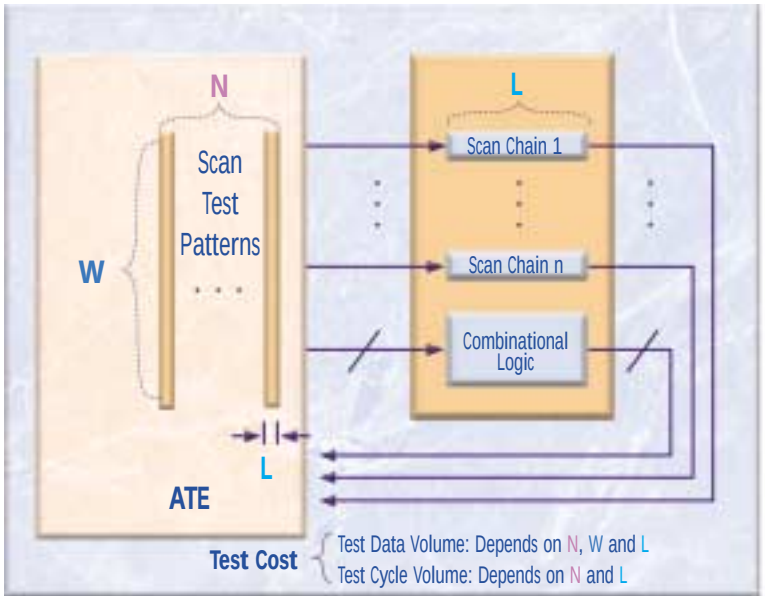
To generate very compact ATPG patterns, SynTest uses proprietary static and dynamic compaction techniques in its ATPG tool.

In static compaction, reverse fault simulation and a minimal cover set algorithm is used to choose the best test pattern which can detect the same hard detected fault list, thereby reducing the total number of test patterns generated.

In dynamic compaction, a proprietary algorithm is used to target secondary faults, while patterns are being generated, until most unknowns in a test pattern are filled-up. This again increases the utilization of the test patterns and consequently reduces the total number of test patterns generated.

Further, SynTest's multiple-capture-per-cycle scheme for ATPG slashes the total test time of designs with multiple-frequency clock domains, as only one scan-in/scan-out phase is deployed for each pattern. Though the multiple-capture-cycle takes a little longer than the capture cycle for schemes based on one-hot clock, it is much shorter than the cumulative time taken by the scan-in and scan-out operations for individual clocks, thereby offering a test compaction factor almost equal to the total number of clock domains.

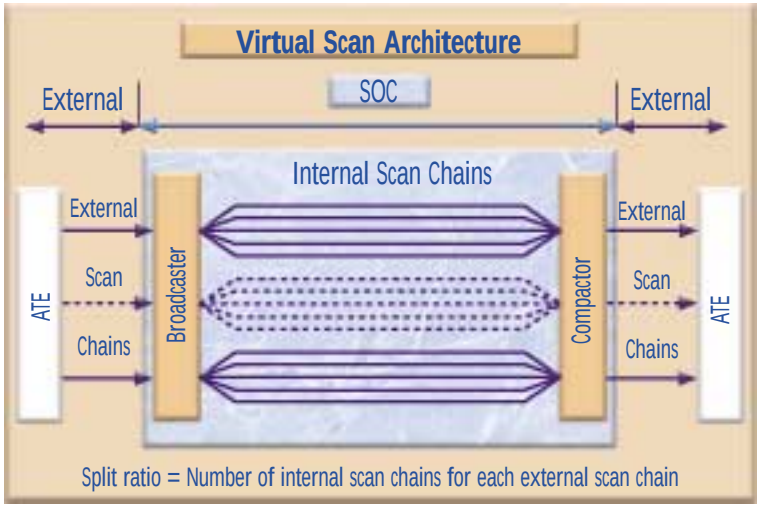
The limitations on the number of scan pins available on an ATE forces longer scan chains to be used for larger and more complex SOC designs.



These longer scan chains obviously take much more time to run on the ATE. Hence, the solution is to be able to use a large number of shorter scan-chains that circumvent the limitation of the number of scan test pins available on the ATE.

With SynTest's VirtualScan™, an extremely large number of short scan chains within the SOC can be virtually accessed from outside the chip with a limited number of ATE pins assigned as scan pins. Inside the chip, SynTest's new patent-pending circuitry is used to broadcast each external scan-input chain to a user-selectable number of internal scan chains and at the other end, compact them into the original number of external scan chains. This helps overcome the limitation on the availability of scan test pins on the ATE.

VirtualScan™ contains an automatic synthesizer to incorporate the broadcaster and compactor into the scan circuitry and uses an enhanced virtual scan ATPG technology to generate test patterns.



VIRTUALSCAN™ – FLOW

The VirtualScan™ flow starts with a synthesized gate-level netlist. SynTest recommends running the netlist through TurboCheck-Gate™. It is a DFT rules violation checker used to check the design after the design is synthesized into gates. It can perform a structural-level check on the final design to identify and zero-in on the final testability violations.

Scan Synthesis

VirtualScan™ contains tools for scan synthesis. It provides scan selection based on clock domains and scan flip-flop count. It automatically repairs testability violations, supports muxed scan, clocked scan, and LSSD (level-sensitive scan design) and performs scan reordering for minimum scan chain routing overhead. A gate-level scan-inserted netlist is generated.

Should you decide to use a tool other than VirtualScan™ for scan synthesis, it is still recommended that the gate-level scan-inserted netlist be tested for DFT violations using TurboCheck-Gate™.

Scan extraction is performed on the gate-level scan-inserted netlist and it is then sent on for the virtual scan configuration.

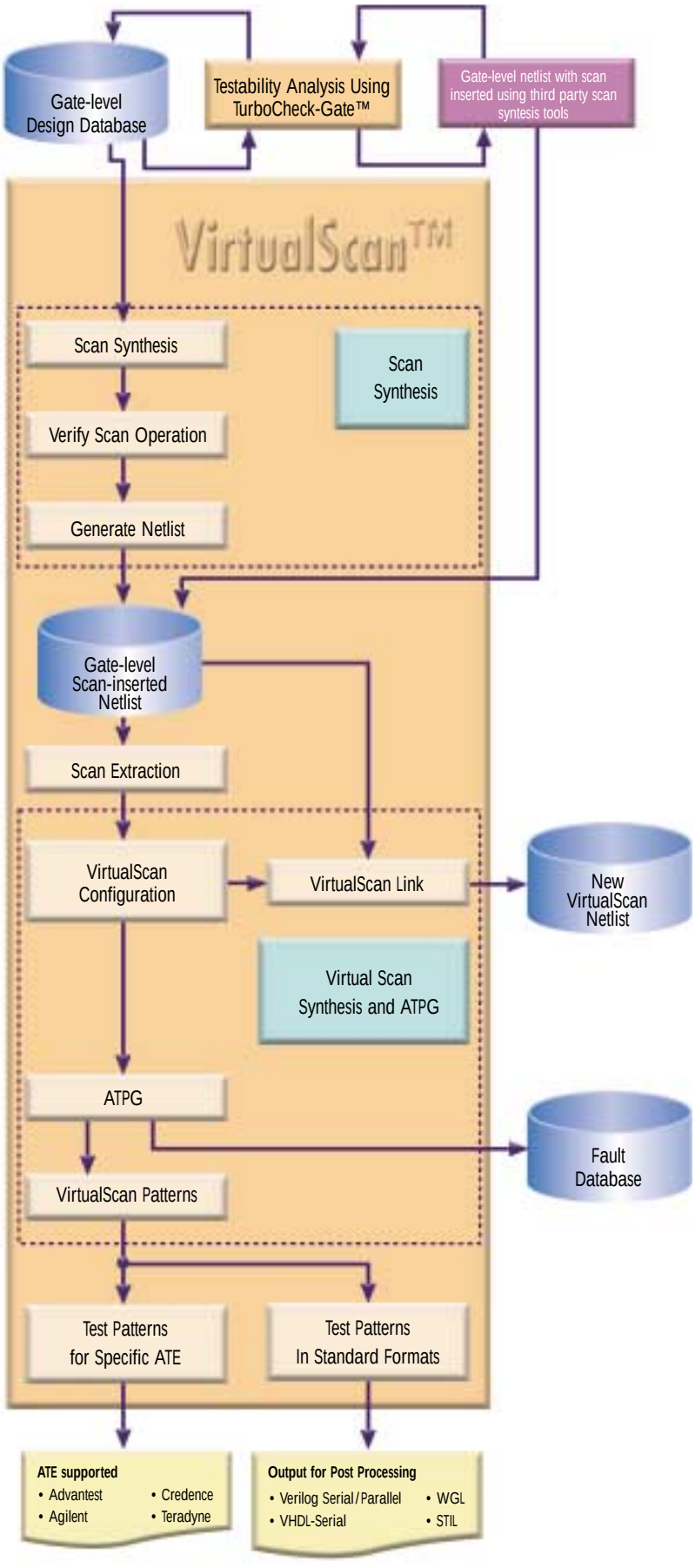
Virtual Scan Synthesis and ATPG

At this stage, an automatic synthesizer incorporates the broadcaster and compactor into the scan circuitry and the scan chains are split into a number of internal scan chains based on the user-definable "Split Ratio". This is then fed to the ATPG tool.

Though VirtualScan™ inserts the broadcaster and compactor into a design, the area impact is extremely small.

The ATPG automatically generates high quality manufacturing test patterns, resulting in a test program used by a specific ATE to test a specific IC device.

The VirtualScan™ ATPG tool uses an enhanced virtual scan ATPG technology to generate test patterns. It also provides a fast combinational and sequential ATPG, which enables very high fault coverage to be achieved.



HOW VIRTUALSCAN™ CAN SAVE TEST COSTS

Example Data from VirtualScan™ Run on a 2-million Gate Design	SCAN ATPG	VirtualScan™ with 0.3% Fault Coverage Loss	VirtualScan™ without Fault Coverage Loss
No. of ATPG Test Patterns	2,659	3,720	4,014(*)
Max Scan Chain Length	3,718	117	3,718
Number of Scan Chains	16	512	16
ATE Test Frequency	10MHz	10MHz	10MHz
Test Data Volume	316,357,184	18,280,080	53,259,024
Test Cycle Volume (Cycles) (**)	9,886,162	435,240	1,528,332
ATE Test Time (Seconds)	0.99	0.04	0.15
Test Cost ($/second)	$0.10	$0.10	$0.10
Device Volume per Year	1,000,000	1,000,000	1,000,000
Total Test Cost per Year	$99,000.00	$4,000.00	$15,000.00
Savings per Year		$95,000.00	$84,000.00
% Savings per Year		95.96%	84.85%

(*) 4,014 = (3720 from VirtualScan + 294 from serial scan)
(**) Test Cycle Volume = ATPG Patterns * Max Scan Chain Length

DEBUG, DIAGNOSIS AND FAILURE ANALYSIS

VirtualScan™ works with SynTest's

- TurboDebug-SOC™/Scan: For PC-based Scan Debugging and Diagnosis
- TurboDiagnosis-Scan™: For ATE-based Scan Diagnosis and Failure Analysis

PLATFORMS

VirtualScan runs on Sun Solaris, HP-UX and Linux operating PCs networked on an UNIX server.

ORDERING INFORMATION

- **VirtualScan™** - Tool Suite for Virtual Scan Synthesis and ATPG (Automatic Test Pattern Generation)

Options

- VirtualScan™ Upgrade: For Existing Licensees of SynTest's TurboScan™
- TurboCheck-Gate™: For Gate-level DFT Rule Checking
- ATE Test Program Outputs
- TurboDebug-SOC™/Scan: For PC-based Scan Debugging and Diagnosis
- TurboDiagnosis-Scan™: For ATE-based Scan Diagnosis and Failure Analysis

Other Products from SynTest

- TurboBSD™: For Boundary-Scan Synthesis
- TurboBIST-Memory™: For Memory-BIST Synthesis
- TurboDFT™: For DFT Integration
- TurboCheck-RTL™: For RTL-level DFT Rule Checking
- TurboBIST-Logic™: Logic BIST Tool Suite
- TurboFault™: For Concurrent Fault Simulation
- TurboDebug-PCB™: For Debugging Interconnects on PCBs
- TurboDebug-SOC/Memory™: For Debugging and Diagnosis of Memory BIST
- TurboDebug-SOC/Logic™: For Debugging and Diagnosis of Logic BIST

VIRTUALSCAN™ – FLOW (CONTINUED)

VirtualScan™ is Engineering-Change-Order (ECO) friendly. In case of an ECO, users just need to re-run ATPG to generate new patterns. Everything else remains the same, including the broadcaster and the compactor. No additional test development effort or test development time is required.

Outputs

The ATPG test patterns are available in various formats for post processing. The standard output formats include Verilog Serial/Parallel, VHDL – Serial, WGL and STIL.

Outputs are also available specifically tailored to match the inputs of ATE from Advantest, Agilent, Credence and Teradyne.

Using the VirtualScan™ Link tool, the original gate-level scan-inserted netlist is converted into a new VirtualScan inserted netlist.

To enhance the fault coverage, the fault database generated can be used to carry out fault grading using TurboFault™, a concurrent fault simulation tool.

Fault Coverage

The most significant feature of VirtualScan™ is that it allows the user to configure it to meet fault coverage requirements.

For example, on a 2-million gate design, running virtual scan mode could result in an extremely small reduction in fault coverage – about 0.3%.

However, to ensure no loss in fault coverage, the user can initially run the ATPG using virtual scan and subsequently run it without virtual scan. Even in this case, significant reductions are available in the test data volume and the test cycle volume.

RELOADS

"Reloads" on an ATE depend on the ATE pattern memory size and the Test Data Volume. Reducing Test Data Volume, reduces the pattern memory size required and the number of "Reloads". See Test Data Volume in the Table "How VirtualScan™ Can Save Test Costs."

INTEGRATION INTO DFT/TEST ENVIRONMENTS

VirtualScan™ is fully compatible with SynTest's existing DFT tools such as TurboBIST-Memory™ for embedded memory BIST, TurboBSD™ for boundary scan synthesis, TurboDFT™ for automatic integration of DFT and IP blocks, and TurboFault™ for concurrent fault simulation.

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