For Immediate Release
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SynTest granted 6 more Patents since October 2006

"Patents portfolio grows to 11 granted plus 2 allowed patents"

SAN JOSE, Calif., July 24, 2007 -- SynTest Technologies, Inc., a leading supplier of Design-for-Test (DFT) tools, has been granted 6 more patents since June 2006 by United States Patent office. These patented inventions cover a wide range of DFT technology applications such as advanced ATPG and pattern compression techniques, Diagnosing failures using Design-for Diagnosis (DFD) Techniques and Analog BIST Methodology. SynTest now has a total of eleven granted patents in the overall patents portfolio.

Three patents have been granted over last one year for advances in the ATPG and pattern compression techniques are: Smart ATPG (U.S. Pat. No. 7,124,342) on October 17, 2006, ATPG and Fault Simulation in a Scan-Based IC (U.S. Pat. No. 7,210,082) on April 24. 2007, Multi-level Scan Compression (U.S. Pat. No. 7,231,570) on June 12, 2007.

Two patents have been granted for advances in the DFT techniques as follows: DFD for scan cores (European Pat. No. 1,364,436), Diagnosing Failures in an IC (U.S. Pat. No. 7,191,373) on March 13, 2007.

One patent has been granted for advances in the Analog BIST techniques as follows: IEEE std. 1149.4 Compatible Analog BIST (U.S. Pat. No. 7,228,479) on June 5, 2007

About SynTest

SynTest Technologies, Inc., established in 1990, develops intellectual properties (IPs) for advanced design-for-test (DFT) and design-for-debug/diagnosis (DFD) applications and licenses them throughout the world, to semiconductor companies, system houses and design service providers. The company has filed for more than 38 US/PCT patents of which 11 have been issued and 2 allowed. The Company's products improve an electronic design's quality and reduce overall design and test costs. Various applications that use these IPs include logic BIST, memory BIST, boundary-scan synthesis, scan/ATPG with test compression, concurrent fault simulation, silicon debug and diagnosis. The company headquartered in Sunnyvale, California, has offices in Taiwan, Japan, Korea and China, and distributors in Europe and Asia including Israel. More information is available at www.syntest.com.

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Acronyms:

ATPG:	Automatic Test Program Generation
BIST:	Built-In Self-Test
DFT:	Design-for-Test
DFD:	Design-for-Debug/Diagnosis
IP:	Intellectual Property
TTM:	Time-to-Market