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SynTest Receives A Fundamental Patent on At-Speed Capture Invention for Scan ATPG

"Multiple-capture DFT system for detecting or locating crossing clock-domain faults during self-test or scan-test"

SAN JOSE, Calif., November 14, 2007 -- SynTest Technologies, Inc., a leading supplier of Design-for-Test (DFT) tools, was granted 79 claims on August 21, 2007 under United States Patent Number 7,260,756 for its invention on At-Speed capture for testing of delay faults in an integrated circuit containing multiple clock domains in the scan ATPG environment.

Dr. L.-T. Wang, founder, president, CEO of SynTest states, "SynTest proprietary technology in this patent has been used to our innovative Scan ATPG products offering (TurboScan and VirtualScan) for many years and is being used by many leading corporations in the world. It is one of the most fundamental patents ever granted by the US Patent Office. This patented approach allows us to help our customers improve quality of the devices they produce today in sub-micron technologies containing multiple clock domains each running at very high frequency or At-Speed. ATPG patterns, created using this patented invention, are most compact patterns which results in significant saving in the test application time on ATE."

"Significant efforts over many years have been applied so far to the development, implementation of the At-Speed capture technology in our products, and in defending the patent application. After application for this patent was made in February 2001, this patent grant after more than 6 years should give DFT community a sense of how fundamental this patent is," added Dr. Ravi Apte, VP of Strategy, Marketing and Business Development of SynTest.

The patented invention are methods and apparatus for providing ordered capture clocks, each running at its intended speed, to detect or locate faults within each clock domain and faults across clock domains in an integrated circuit in scan ATPG test mode, where each

domain has scan chains. Dubbed "staggered launch-on-capture" or "staggered double-capture", the capture-clocking scheme allows designs containing synchronous and asynchronous clock domains to perform at-speed scan ATPG test. SynTest TurboScan and VirtualScan test compression products are based on this technology invention. A slow Scan-Enable control signal, commonly used for slow-speed test, is also used for at-speed scan testing using this patented invention. Use of this patented invention results in improved productivity and time-to-market (TTM). Since without it, only "one-hot" clock method can be used for at-speed scan testing resulting in significant increase in test application time on ATE (proportional to number of clock domains in the design) and subsequent significant increase in overall test cost.

About SynTest

SynTest Technologies, Inc., established in 1990, develops IP for advanced design-for-test (DFT) and design-for-debug/diagnosis (DFD) applications and markets them throughout the world, to semiconductor companies, system houses and design service providers. The company has filed more than 38 US/PCT patents of which 13 have been issued and 2 allowed. The Company's products improve an electronic design's quality and reduce overall design and test costs. Various applications that use these IP (intellectual properties) include logic BIST, memory BIST, boundary-scan synthesis, Scan/ATPG with test compression, concurrent fault simulation, silicon debug and diagnosis. The company headquartered in Sunnyvale, California, has offices in Taiwan, Japan, Korea and China, and distributors in Europe and Asia including Israel. More information is available at www.syntest.com.

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Acronyms:

ATPG: Automatic Test Pattern Generation
ATE: Automatic Test Equipment
BIST: Built-In Self-Test
DFT: Design-for-Test

DFD: Design-for-Debug/Diagnosis
IP: Intellectual Property
TTM: Time-to-Market